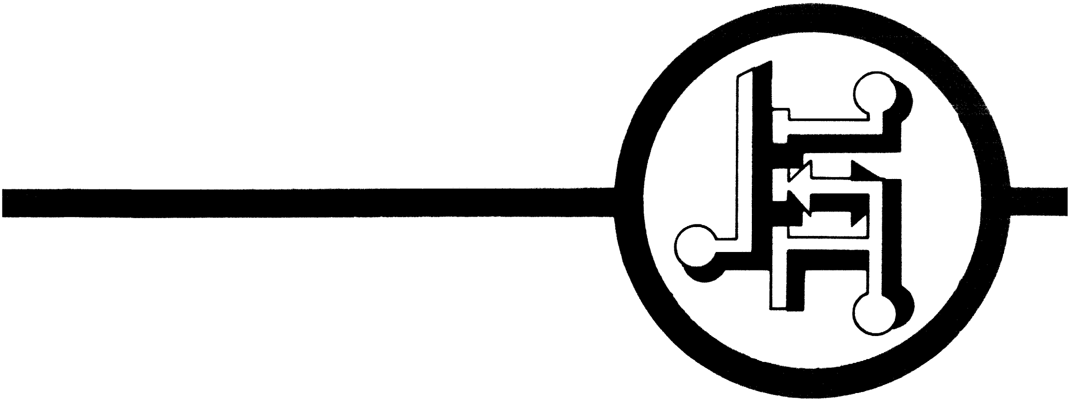
Technical Handbook
1991

MOSFETS



ZETEX

Zetex is the largest UK-owned specialist discrete semiconductor manufacturer. Freed from the constraints of a large integrated company — after a recent management-led buy-out — Zetex (formerly Ferranti) can focus more closely on meeting marketing needs.

The company, now in industrial partnership with Telemetrix, provides the best possible discrete components technology and service — all too often a low priority to other semiconductor manufacturers.

Products are based on bipolar and MOSFET chip technology offered in a variety of assemblies suitable for either thru-hole or surface mount applications, for example our Super E-line and SOT-23 ranges, which offer exceptional performance in compact packages.

Zetex's 60,000 square feet production area features class 100 clean rooms with SPC, ESD and PPM programs in place to ensure consistent product quality. All this is now backed up by a dedicated sales and marketing team including full technical and applications support.

For more information on the company and its products, contact your nearest sales office or agent.

Publication No. Z1067 January 1991

CONTENTS

NUMERIC-ALPHA PRODUCT INDEX

It is the intention of Zetex to phase out voltage downgrades from its MOSFET range. Support will be given to all existing design-ins. In the interim, parts lists should be updated to include the prime types. The following product listing, indicating the devices to refer to, has been generated to assist in this task.

PRODUCT INDEX

Previous part No.	Refer to	Selection table No.	Data sheet page No.
2N7000	2N7000	1	F-3
2N7002	2N7002	4	F-5
BS107P	BS107P	1	F-7
BS107PT	BS107PT	1	F-15
BS170F	BS170F	4	F-23
BS170P	BS170P	1	F-23
BS250F	BS250F	4	F-31
BS250P	BS250P	2	F-39
BSS84	BSS84	4	F-47
BSS123	BSS123	4	F-49
BSS138	BSS138	4	F-51
VN10LF	VN10LF	4	F-53
VN10LP	VN10LP	1	F-53
ZVNL110A	ZVNL110A	3	F-61
ZVNL120A	ZVNL120A	3	F-63
ZVNL120C	ZVNL120C	6	F-63
ZVNL535A	ZVNL535A	3	F-71
ZVN0102A	ZVN2106A	1	F-117
ZVN0102B	ZVN2106B	1	F-117
ZVN0104A	ZVN2110A	1	F-125
ZVN0106A	ZVN2110A	1	F-125
ZVN0106B	ZVN2110B	1	F-125
ZVN0117TA	ZVN0117TA	1	F-73
ZVN0120A	ZVN0120A	1	F-81
ZVN0120B	ZVN0120B	1	F-81
ZVN0124A	ZVN0124A	1	F-89
ZVN0124B	ZVN0124B	1	F-89
ZVN0530A	ZVN0535A	1	F-97
ZVN0530B	ZVN2535B	1	F-141
ZVN0535A	ZVN0535A	1	F-97
ZVN0535B	ZVN2535B	1	F-141
ZVN0540A	ZVN0540A	1	F-105
ZVN0540B	ZVN0540B	1	F-105
ZVN0545A	ZVN0545A	1	F-107
ZVN0545B	ZVN0545B	1	F-107
ZVN1306A	ZVN3310A	1	F-157
ZVN1306B	ZVN3310B	1	F-157
ZVN1306F	ZVN3310F	4	F-157
ZVN1308A	ZVN3310A	1	F-157
ZVN1308B	ZVN3310B	1	F-157
ZVN1308F	ZVN3310F	4	F-157

Previous part No.	Refer to	Selection table No.	Data sheet page No.
ZVN1320A	ZVN3320A	1	F-165
ZVN1320B	ZVN3320B	1	F-165
ZVN1320F	ZVN3320F	4	F-165
ZVN1404A	ZVN1409A	1	F-109
ZVN1406A	ZVN1409A	1	F-109
ZVN1408A	ZVN1409A	1	F-109
ZVN1409A	ZVN1409A	1	F-109
ZVN2104A	ZVN2106A	1	F-117
ZVN2104B	ZVN2106B	1	F-117
ZVN2106A	ZVN2106A	1	F-117
ZVN2106B	ZVN2106B	1	F-117
ZVN2106E	ZVN2106E	5	F-117
ZVN2106G	ZVN2106G	7	F-117
ZVN2110A	ZVN2110A	1	F-125
ZVN2110B	ZVN2110B	1	F-125
ZVN2110C	ZVN2110C	6	F-125
ZVN2110E	ZVN2110E	5	F-125
ZVN2117A	ZVN2120A	1	F-133
ZVN2117B	ZVN2120B	1	F-133
ZVN2120A	ZVN2120A	1	F-133
ZVN2120B	ZVN2120B	1	F-133
ZVN2120C	ZVN2120C	6	F-133
ZVN2535A	ZVN2535A	1	F-141
ZVN2535B	ZVN2535B	1	F-141
ZVN3302A	ZVN3306A	1	F-149
ZVN3302B	ZVN3306B	1	F-149
ZVN3302F	ZVN3306F	4	F-149
ZVN3304A	ZVN3306A	1	F-149
ZVN3304B	ZVN3306B	1	F-149
ZVN3304F	ZVN3306F	4	F-149
ZVN3306A	ZVN3306A	1	F-149
ZVN3306B	ZVN3306B	1	F-149
ZVN3306E	ZVN3306E	5	F-149
ZVN3306F	ZVN3306F	4	F-149
ZVN3310A	ZVN3310A	1	F-157
ZVN3310B	ZVN3310B	1	F-157
ZVN3310F	ZVN3310F	4	F-157
ZVN3315A	ZVN3320A	1	F-165
ZVN3315B	ZVN3320B	1	F-165
ZVN3315F	ZVN3320F	4	F-165

PRODUCT INDEX

Previous part No.	Refer to	Selection table No.	Data sheet page No.
ZVN3320A	ZVN3320A	1	F-165
ZVN3320B	ZVN3320B	1	F-165
ZVN3320F	ZVN3320F	4	F-165
ZVN4106F	ZVN4106F	4	F-167
ZVN4206A	ZVN4206A	1	F-175
ZVN4206C	ZVN4206C	6	F-175
ZVN4206E	ZVN4206E	5	F-175
ZVP0102A	ZVP2106A	2	F-211
ZVP0102B	ZVP2106B	2	F-211
ZVP0106A	ZVP2110A	2	F-219
ZVP0106B	ZVP2110B	2	F-219
ZVP0108A	ZVP2110A	2	F-219
ZVP0108B	ZVP2110B	2	F-219
ZVP0120A	ZVP0120A	2	F-183
ZVP0120B	ZVP0120B	2	F-183
ZVP0530A	ZVP0535A	2	F-191
ZVP0530B	ZVP0535B	2	F-191
ZVP0535A	ZVP0535A	2	F-191
ZVP0535B	ZVP0535B	2	F-191
ZVP0540A	ZVP0540A	2	F-199
ZVP0540B	ZVP0540B	2	F-199
ZVP0545A	ZVP0545A	2	F-201
•ZVP0545B	ZVP0545B	2	F-201
ZVP1306A	ZVP3310A	2	F-243
ZVP1306B	ZVP3310B	2	F-243
ZVP1306F	ZVP3310F	4	F-243
ZVP1308A	ZVP3310A	2	F-243
ZVP1308B	ZVP3310B	2	F-243
ZVP1308F	ZVP3310F	4	F-243
ZVP1320A	ZVP1320A	2	F-203
ZVP1320B	ZVP1320B	2	F-203
ZVP1320F	ZVP1320F	4	F-203
ZVP2104A	ZVP2106A	2	F-211
ZVP2104B	ZVP2106B	2	F-211
ZVP2106A	ZVP2106A	2	F-211
ZVP2106B	ZVP2106B	2	F-211
ZVP2106C	ZVP2106C	6	F-211
ZVP2106E	ZVP2106E	5	F-211
ZVP2106G	ZVP2106G	7	F-211

Previous part No.	Refer to	Selection table No.	Data sheet page No.
ZVP2110A	ZVP2110A	2	F-219
ZVP2110B	ZVP2110B	2	F-219
ZVP2110C	ZVP2110C	6	F-219
ZVP2110E	ZVP2110E	5	F-219
ZVP2120A	ZVP2120A	2	F-227
ZVP2120B	ZVP2120B	2	F-227
ZVP2120C	ZVP2120C	6	F-227
ZVP3302A	ZVP3306A	2	F-235
ZVP3302B	ZVP3306B	2	F-235
ZVP3302F	ZVP3306F	4	F-235
ZVP3304A	ZVP3306A	2	F-235
ZVP3304B	ZVP3306B	2	F-235
ZVP3304F	ZVP3306F	4	F-235
ZVP3306A	ZVP3306A	2	F-235
ZVP3306B	ZVP3306B	2	F-235
ZVP3306E	ZVP3306E	5	F-235
ZVP3306F	ZVP3306F	4	F-235
ZVP3310A	ZVP3310A	2	F-243
ZVP3310B	ZVP3310B	2	F-243
ZVP3310F	ZVP3310F	4	F-243
ZVP3315A	ZVP1320A	2	F-203
ZVP3315B	ZVP1320B	2	F-203
ZVP3315F	ZVP1320F	4	F-203
ZVP4105A	ZVP4105A	2	F-251

NUMERIC-ALPHA
CROSS REFERENCE LIST

CROSS REFERENCE

Industry part No.	Zetex suggested replacement	Data sheet page No.
2N6659	ZVN2106B	F-117
2N6660	ZVN2106B	F-117
2N6661	ZVN2110B	F-125
2N7000	2N7000	F-3
2N7001	ZVN3320F	F-165
2N7002	2N7002	F-5
2N7007	ZVN3320A	F-165
2N7008	ZVN3306A	F-149
2N7019	ZVP3306F	F-235
2N7025	ZVP2106A	F-211
AM0610LL	VN10LP	F-53
AM2222LL	VN10LP	F-53
AM7000	2N7000	F-3
AM7008	2N7000	F-3
BS107	BS107P	F-7
BS107A	ZVNL120A	F-63
BS108	ZVNL120A	F-63
BS170	BS170P	F-23
BS250	BS250P	F-39
BSR64	VN10LP	F-53
BSR65	VN10LP	F-53
BSR66	ZVN2106A	F-117
BSR67	ZVN2110A	F-125
BSR70	ZVNL120A	F-63
BSR72	ZVNL120A	F-63
BSR76	ZVNL120A	F-63
BSR78	ZVP2106A	F-211
BSS84	BSS84	F-47
BSS87	ZVNL120CSM	F-63
BSS88	ZVN2120C	F-133
BSS89	ZVN2120C	F-133
BSS91	ZVN2120B	F-133
BSS92	ZVP2120C	F-227
BSS100	ZVN2110A	F-125
BSS101	ZVN2120A	F-133
BSS110	ZVP2106A	F-211
BSS123	BSS123	F-49
BSS138	BSS138	F-51
BST70A	ZVN2110A	F-125
BST72A	ZVN3310A	F-157
BST74A	ZVN2120A	F-133
BST76A	ZVN2120A	F-133
BST80	ZVN2110CSM	F-125
BST82	ZVN3310F	F-157
BST84	ZVN2120CSM	F-133
BST86	ZVNL120CSM	F-63
BST90	ZVN2110B	F-125
BST97	ZVN2120B	F-133
BST100	ZVP2106A	F-211
BST110	ZVP2106A	F-211
BST120	ZVP2106CSM	F-211
D80AK1	ZVN2106A	F-117
D80AK2	ZVN2106A	F-117

Industry part No.	Zetex suggested replacement	Data sheet page No.
MFE910	ZVN3306B	F-149
MFE930	ZVN2106B	F-117
MFE960	ZVN2106B	F-117
MFE990	ZVN2110B	F-125
MFQ930P	ZVN4206E	F-175
MFQ960P	ZVN2106E	F-117
MFQ1000P	ZVN2106E	F-117
MFQ6659P	ZVN4206E	F-175
MFQ6661P	ZVN2110E	F-125
MMBF170L	BS170F	F-23
MPF910	ZVN3306A	F-149
MPF930	ZVN4206A	F-175
MPF960	ZVN4206A	F-175
MPF990	ZVN2110A	F-125
MPF6659	ZVN4206A	F-175
MPF6660	ZVN2106A	F-117
MPF6661	ZVN2110A	F-125
MPF89	ZVN2120A	F-133
MPF9200	ZVN2120A	F-133
PH6659	ZVN2106A	F-117
PH6660	ZVN2106A	F-117
PH6661	ZVN2110A	F-125
PMBF170	BS170F	F-23
TN0106N3	ZVNL110A	F-61
TN0110N3	ZVNL110A	F-61
TN0520N3	ZVNL120A	F-63
TP0610L	ZVP4105A	F-251
TP0610T	BSS84	F-47
VN10KMA	VN10LP	F-53
VN10KN3	VN10LP	F-53
VN10LE	VN10LP	F-53
VN10LM	VN10LP	F-53
VN35AB	ZVN2106B	F-117
VN40AF	ZVN2106A	F-117
VN46AF	ZVN2106A	F-117
VN66AF	ZVN2106A	F-117
VN67AB	ZVN2106B	F-117
VN67AF	ZVN2106A	F-117
VN80AF	ZVN2110A	F-125
VN88AF	ZVN2110A	F-125
VN89AF	ZVN2110A	F-125
VN90AB	ZVN2110B	F-125
VN99AB	ZVN2110B	F-125
VN0104N2	ZVN2106B	F-117
VN0104N3	ZVN2106A	F-117
VN0104N6	ZVN2106E	F-117
VN0106N2	ZVN2106B	F-117
VN0106N3	ZVN2106A	F-117
VN0106N6	ZVN2106E	F-117
VN0109N2	ZVN2110B	F-125
VN0109N3	ZVN2110A	F-125
VN0116N2	ZVN2120B	F-133
VN0116N3	ZVN2120A	F-133
VN0120N2	ZVN2120B	F-133
VN0120N3	ZVN2120A	F-133

CROSS REFERENCE

Industry part No.	Zetex suggested replacement	Data sheet page No.
VN0204N6	ZVN4206E	F-175
VN0206N3	ZVN4206A	F-175
VN0206N6	ZVN4206E	F-175
VN0216N3	ZVNL120A	F-63
VN0220N3	ZVNL120A	F-63
VN0300B	ZVN2106B	F-117
VN0300L	ZVN4206A	F-175
VN0300M	ZVN4206A	F-175
VN0535N2	ZVN2535B	F-141
VN0535N3	ZVN2535A	F-141
VN0540N2	ZVN0540B	F-105
VN0540N3	ZVN0540A	F-105
VN0545N2	ZVN0545B	F-107
VN0545N3	ZVN0545A	F-107
VN0603L	ZVN2106A	F-117
VN0603T	ZVN4106F	F-167
VN0605T	ZVN3306F	F-149
VN0606L	ZVN2106A	F-117
VN0606M	ZVN2106A	F-117
VN0610LL	VN10LP	F-53
VN0808L	ZVNL110A	F-61
VN0808M	ZVNL110A	F-61
VN1206B	ZVN2110B	F-125
VN1206L	ZVN2110A	F-125
VN1206M	ZVN2110A	F-125
VN1210L	ZVN3310A	F-157
VN1210M	ZVN3310A	F-157
VN1304N2	ZVN3306B	F-149
VN1304N3	ZVN3306A	F-149
VN1306N2	ZVN3306B	F-149
VN1306N3	ZVN3306A	F-149
VN1306N6	ZVN3306E	F-149
VN1310N2	ZVN3310B	F-157
VN1310N3	ZVN3310A	F-157
VN1316N2	ZVN3320B	F-165
VN1316N3	ZVN3320A	F-165
VN1320N2	ZVN3320B	F-165
VN1320N3	ZVN3320A	F-165
VN1706B	ZVN2120B	F-133
VN1706L	ZVNL120A	F-63
VN1706M	ZVNL120A	F-63
VN1710L	ZVNL120A	F-63
VN1710M	ZVNL120A	F-63
VN1720M	ZVNL120A	F-63
VN2010L	ZVNL120A	F-63
VN2020L	ZVN0120A	F-81
VN2222LL	VN10LP	F-53
VN2222LM	VN10LP	F-53
VN2406L	ZVNL120A	F-63
VN2406M	ZVNL120A	F-63
VN2410L	ZVNL120A	F-63
VN2410M	ZVNL120A	F-63
VN2420L	ZVN0124A	F-89

Industry part No.	Zetex suggested replacement	Data sheet page No.
VN45350L	ZVN0545A	F-107
VP0104N2	ZVP2106B	F-211
VP0104N3	ZVP2106A	F-211
VP0104N6	ZVP2106E	F-211
VP0106N2	ZVP2106B	F-211
VP0106N3	ZVP2106A	F-211
VP0106N6	ZVP2106E	F-211
VP0109N2	ZVP2110B	F-219
VP0109N3	ZVP2110A	F-219
VP0116N2	ZVP2120B	F-227
VP0116N3	ZVP2120A	F-227
VP0120N2	ZVP2120B	F-227
VP0120N3	ZVP2120A	F-227
VP0204N6	ZVP2106E	F-211
VP0206N3	ZVP2106A	F-211
VP0206N6	ZVP2106E	F-211
VP0300B	ZVP2106B	F-211
VP0300L	ZVP2106A	F-211
VP0300M	ZVP2106A	F-211
VP0535N2	ZVP0535B	F-191
VP0535N3	ZVP0535A	F-191
VP0540N2	ZVP0540B	F-199
VP0540N3	ZVP0540A	F-199
VP0545N2	ZVP0545B	F-201
VP0545N3	ZVP0545A	F-201
VP0610L	ZVP3306A	F-235
VP0610T	ZVP3306F	F-235
VP0808B	ZVP2110B	F-219
VP0808L	ZVP2110A	F-219
VP0808M	ZVP2110A	F-219
VP1008B	ZVP2110B	F-219
VP1008L	ZVP2110A	F-219
VP1008M	ZVP2110A	F-219
VP1304N2	ZVP3306B	F-235
VP1304N3	ZVP3306A	F-235
VP1306N2	ZVP3306B	F-235
VP1306N3	ZVP3306A	F-235
VP1306N6	ZVP3306E	F-235
VP1310N2	ZVP3310B	F-243
VP1310N3	ZVP3310A	F-243
VP1316N2	ZVP1320B	F-203
VP1316N3	ZVP1320A	F-203
VP1320N2	ZVP1320B	F-203
VP1320N3	ZVP1320A	F-203
VQ1000J	ZVN3306E	F-149
VQ1001J	ZVN4206E	F-175
VQ1004J	ZVN2106E	F-117
VQ1006J	ZVN2110E	F-125
VQ2000J	ZVP3306E	F-235
VQ2001J	ZVP2106E	F-211
VQ2004J	ZVP2106E	F-211
VQ2006J	ZVP2110E	F-219

ZETEX MOSFET TECHNOLOGY

MOSFET Technology

Introduction

Zetex MOSFET technology is amongst the world's most advanced. Its MOSFETs are enhancement mode devices (normally off) especially suited to a wide range of switching and amplifying applications where high gain, high frequency and fast switching speed is desired. They combine the current handling capabilities of bipolar transistors with the high input impedance and negative temperature coefficients of FETs.

Having considered the various MOSFET technologies available (ie V groove, U groove, DMOS) Zetex has adopted a vertical DMOS structure. The advantages of this structure over the others considered may be summarised as:

- Short channel lengths determined by an easily controlled diffusion process for lower on-resistance and increased current density.
- Planar construction simplifies wafer fabrication due to the elimination of etched grooves
- Increased conductance per unit area
- Improved high voltage capability
- Both N and P-channel devices can be easily fabricated
- Compact metallisation for reduced chip size

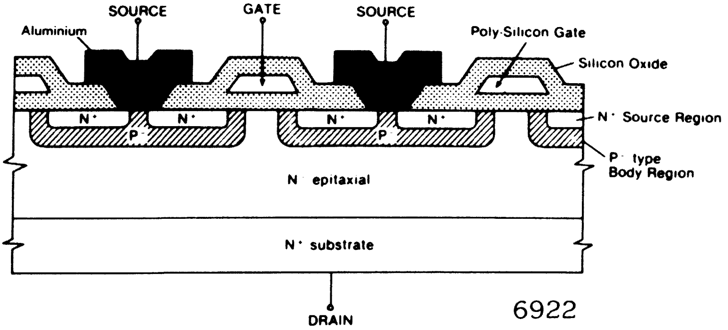
An abundance of terms already exist for individual manufacturers versions of the basic vertical DMOS process eg. HEXFET®, SIPMOS®, TMOS® the main differences being the geometry of the N-type and P-type regions and the interconnections.

Vertical DMOS devices can be fabricated with either an interdigitated or cell geometry.

ZETEX DMOS PROCESS

Taking an N-channel device as an example. An N^- epitaxial layer is grown on an N^+ substrate. Next a series of P^- body regions are diffused into the epitaxial layer and a poly-silicon gate is embedded in the silicon oxide insulating layer. Source and gate metallisations are deposited on the top surface of the dice and the drain contact made to the bottom surface.

The vertical DMOS process may be considered truly planar as both source and body regions are diffused through a window opened in the poly-silicon layer, without grooves of any kind.



Cross-section of Zetex vertical DMOS process

Both N and P channel devices utilise the vertical DMOS process. It should be realised, however, that since the resistivity of P-type silicon is much higher than that of an N-type silicon, a P-channel device will require a larger active area to achieve the same on-resistance and current rating. The larger area will mean that parameters related to die area will be different; preventing symmetry in this respect.

MOSFET Technology

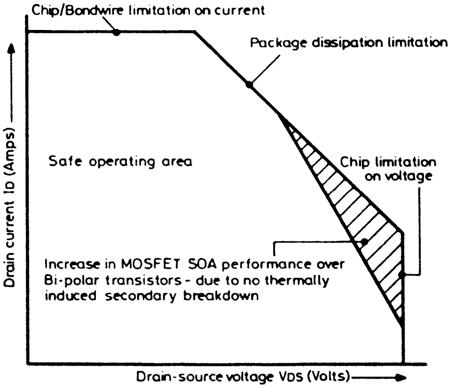
PROCESS HIGHLIGHTS

● Poly-silicon gate process	The poly-silicon gate greatly reduces the possibility of sodium-ion contamination in the gate oxide giving high stability of threshold voltage.
● Ion implantation	The use of ion implantation gives stability in the control of threshold voltages in manufacture.
● Self-aligned gate	The self-aligned DMOS process allows extremely short channel lengths to be achieved, giving these devices excellent linear transfer characteristics.
● Planar construction	The vertical DMOS structure eliminates the need for an isotropically etched V or U-grooves in the surface of the device, giving improved performance and higher voltages.
● Compact geometries	Compact transistor chip designs, utilising interdigitated or cell structures optimised for low on-resistance, low capacitance and fast switching speed.

MOSFET Characteristics

THERMAL RUNAWAY

The devices do not exhibit thermal runaway or thermally induced secondary breakdown.



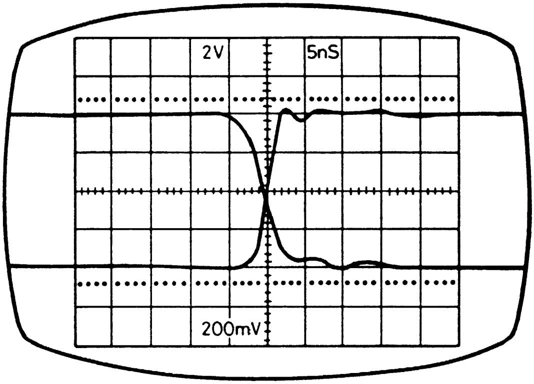
Carrier mobility in a MOSFET channel region decreases with temperature. If localized heating occurs in a MOSFET the carrier mobility decreases in the region affected, and as a consequence, the localized current reduces. This negative feedback mechanism forces overload currents to be uniformly distributed within the transistor.

TEMPERATURE STABILITY

The transconductance and switching times of these MOSFETs change very little with temperature compared to bipolar transistors.

FAST SWITCHING SPEEDS

MOSFETs are majority-carrier devices, and consequently do not exhibit minority carrier storage delays. Switching times are ultra-fast, primarily being determined by the device capacitances and the drive circuitry.



TYPICAL MOSFET SWITCHING CHARACTERISTIC

MOSFET Characteristics

HIGH INPUT IMPEDANCE

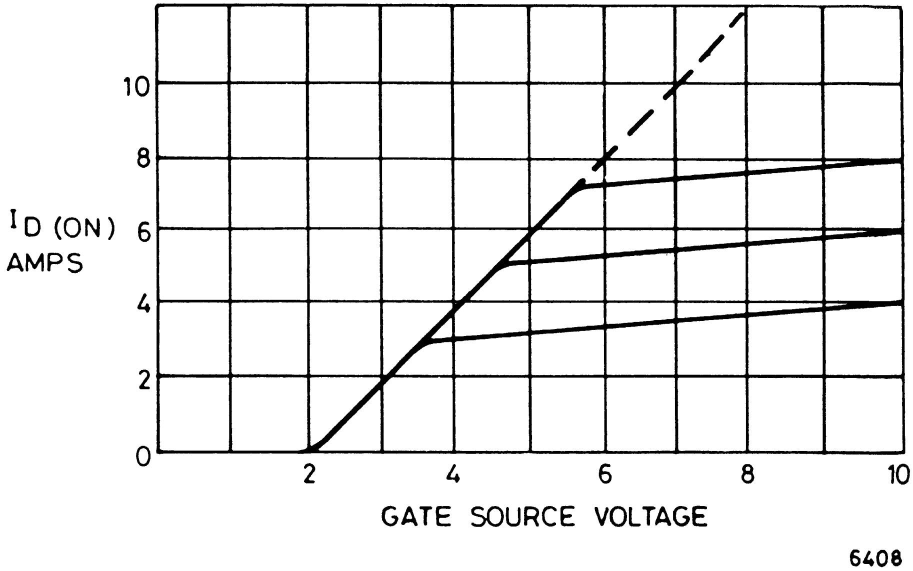
By virtue of the insulated gate structure, input currents are very low, typically a few pico amps at 25°C.

HIGH GAIN

Current gains are generally in the range 10^5 to 10^6.

LINEARITY OF TRANSFER CHARACTERISTICS

Above the threshold voltage, the relationship between drain current and gate voltage in these short channel devices is approximately linear. In other words, the device transconductance, which is the rate of change of drain current with gate voltage, becomes constant at high drain currents.



TYPICAL MOSFET TRANSFER CHARACTERISTICS

PRODUCT ADVANTAGES FOR CIRCUIT DESIGN

1. Less peripheral components are required than in the case of bipolar types leading to reduced design time, less complexity and lower cost.

2. Can be easily connected in parallel to obtain very high current handling performance without the problem related to bipolar transistors, that of base current sharing resistors.

3. Improved reliability due to temperature stability and freedom from thermally induced secondary breakdown.

MOSFET Applications

I.C. Logic Interface Driver

The high input impedance and high power gain make these devices ideally suited as direct interfaces for microprocessor and standard logic e.g. CMOS, TTL, PMOS and NMOS.

Analogue Switching

The output resistance can be switched from very high to very low values with minimal input power bringing design advantages for controlled variable resistance, analogue switching and controlled current sources.

Audio Amplification

The linearity of the transfer characteristics coupled with the fast switching speed gives improved designs in Class A operation, Class D operation and Push-pull audio outputs using complementary types.

Control Circuits

Pulse modulation systems utilise the characteristics of high power gain, speed and thermal stability in d.c. motor speed control, a.c. motor speed control and Stepping motor control.

Sensor Applications

The high input resistance and high power gain enable the devices to be used in sample and hold circuits, touch sensitive circuits, and battery operation – standby power minimal.

Power Supply Circuits

The fast switching speeds, temperature stability, and freedom from thermally induced secondary breakdown of these devices are outstanding characteristics desirable in the areas of switch mode power supplies, d.c./d.c. conversion, and regulation.

Timing Circuits

The input, consisting of capacitance shunted by high input resistance, is ideal for circuits using RC timing components such as pulse and industrial timers, delay circuits, flashing indicators and other types of periodic pulsing applications.

Switching

The fast switching speeds, temperature stability, and freedom from thermally induced secondary breakdown are desirable for very fast pulse generators, filament lamp drivers and laser diode drivers.

Frequency Amplification

The high frequency bandwidth gives amplification from d.c. to hundreds of megahertz allowing useage in radio frequency power stages up to and including communication bands, ultra sonic power stages and high frequency drivers of L.E.D's and laser diodes in fibre optic systems.

Telecommunications

Freedom from thermally induced secondary breakdown is an essential requirement for hook switches and pulsed dialing functions. High gain and low capacitances make the devices ideal for power supply and signal switching.

PRODUCT SELECTION TABLES

SELECTION TABLES

TABLE 1: N-CHANNEL SMALL SIGNAL MOSFETS

Part number	BV_{DSS}	I_D	I_{DM}	$V_{GS(th)}$ V		at I_D	$R_{DS(on)}$ Ω	at I_D	V_{GS}	P_D	Package
	V	mA	A	Min.	Max.	mA	Max.	mA	V	W	
ZVN0545A*	450	90	0.6	1	3	1	50	100	10	0.7	E-line
ZVN0545B	450	150	0.6	1	3	1	50	100	10	5	TO-39
ZVN0540A*	400	90	0.6	1	3	1	50	100	10	0.7	E-line
ZVN0540B	400	150	0.6	1	3	1	50	100	10	5	TO-39
ZVN2535A	350	90	1	1	3	1	35	100	10	0.7	E-line
ZVN2535B	350	250	1	1	3	1	35	100	10	5	TO-39
ZVN0535A*	350	90	0.6	1	3	1	50	100	10	0.7	E-line
ZVN0124A	240	160	2	1	3	1	16	250	10	0.7	E-line
ZVN0124B	240	420	2	1	3	1	16	250	10	5	TO-39
ZVN2120A	200	180	2	1	3	1	10	250	10	0.7	E-line
ZVN2120B	200	460	2	1	3	1	10	250	10	5	TO-39
BS107P	200	120	2	–	–	–	23	25	2.6	0.5	E-line
BS107PT	200	120	2	–	–	–	28	20	2.6	0.5	E-line
ZVN0120A	200	160	2	1	3	1	16	250	10	0.7	E-line
ZVN0120B	200	420	2	1	3	1	16	250	10	5	TO-39
ZVN3320A	200	100	1	1	3	1	25	100	10	0.625	E-line
ZVN3320B	200	250	1	1	3	1	25	100	10	5	TO-39
ZVN0117TA	170	160	2	–	–	–	23	100	3.3	0.7	E-line
ZVN2110A*	100	320	6	0.8	2.4	1	4	1000	10	0.7	E-line
ZVN2110B*	100	850	6	0.8	2.4	1	4	1000	10	5	TO-39
ZVN3310A	100	200	2	0.8	2.4	1	10	500	10	0.625	E-line
ZVN3310B	100	500	2	0.8	2.4	1	10	500	10	5	TO-39
ZVN1409A§	90	10	0.04	0.8	2.4	0.1	250	5	10	0.625	E-line
ZVN4206A	60	600	8	1.3	3	1	1	1500	10	0.7	E-line
ZVN2106A*	60	450	8	0.8	2.4	1	2	1000	10	0.7	E-line
ZVN2106B*	60	1200	8	0.8	2.4	1	2	1000	10	5	TO-39
2N7000	60	200	0.5	0.8	3	1	5	500	10	0.4	E-line
ZVN3306A	60	270	3	0.8	2.4	1	5	500	10	0.625	E-line
ZVN3306B	60	750	3	0.8	2.4	1	5	500	10	5	TO-39
VN10LP	60	270	3	0.8	2.5	1	7.5	200	5	0.625	E-line
BS170P	60	270	3	0.8	3	1	5	200	10	0.625	E-line

*BS-CECC approved §Low input and feedback capacitance device

SELECTION TABLES

TABLE 2: P-CHANNEL SMALL SIGNAL MOSFETS

Part number	BV_{DSS}	I_D	I_{DM}	$V_{GS(th)}$ V		at I_D	$R_{DS(on)}$ Ω	at I_D	V_{GS}	P_D	Package
	V	mA	A	Min.	Max.	mA	Max.	mA	V	W	
ZVP0545A	-450	-45	-0.4	-1.5	-4.5	-1	150	-50	-10	0.7	E-line
ZVP0545B	-450	-100	-0.4	-1.5	-4.5	-1	150	-50	-10	5	TO-39
ZVP0540A	-400	-45	-0.4	-1.5	-4.5	-1	150	-50	-10	0.7	E-line
ZVP0540B	-400	-100	-0.4	-1.5	-4.5	-1	150	-50	-10	5	TO-39
ZVP0535A	-350	-50	-0.48	-1.5	-4.5	-1	100	-50	-10	0.7	E-line
ZVP0535B	-350	-120	-0.48	-1.5	-4.5	-1	100	-50	-10	5	TO-39
ZVP2120A	-200	-120	-1.2	-1.5	-3.5	-1	25	-150	-10	0.7	E-line
ZVP2120B	-200	-300	-1.2	-1.5	-3.5	-1	25	-150	-10	5	TO-39
ZVP0120A	-200	-110	-1	-1.5	-3.5	-1	32	-125	-10	0.7	E-line
ZVP0120B	-200	-250	-1	-1.5	-3.5	-1	32	-125	-10	5	TO-39
ZVP1320A	-200	-70	-0.4	-1.5	-3.5	-1	80	-50	-10	0.625	E-line
ZVP1320B	-200	-100	-0.4	-1.5	-3.5	-1	80	-50	-10	5	TO-39
ZVP2110A*	-100	-230	-3	-1.5	-3.5	-1	8	-375	-10	0.7	E-line
ZVP2110B*	-100	-600	-3	-1.5	-3.5	-1	8	-375	-10	5	TO-39
ZVP3310A	-100	-140	-1.2	-1.5	-3.5	-1	20	-150	-10	0.625	E-line
ZVP3310B	-100	-300	-1.2	-1.5	-3.5	-1	20	-150	-10	5	TO-39
ZVP2106A*	-60	-280	-4	-1.5	-3.5	-1	5	-500	-10	0.7	E-line
ZVP2106B*	-60	-760	-4	-1.5	-3.5	-1	5	-500	-10	5	TO-39
ZVP3306A	-60	-160	-1.6	-1.5	-3.5	-1	14	-200	-10	0.625	E-line
ZVP3306B	-60	-400	-1.6	-1.5	-3.5	-1	14	-200	-10	5	TO-39
ZVP4105A	-50	-175	-0.52	-0.8	-2.0	-1	10	-100	-5	0.625	E-line
BS250P	-45	-230	-3	-1	-3.5	-1	14	-200	-10	0.7	E-line

* BS-CECC approved

TABLE 3: LOW THRESHOLD MOSFETS

Part number	BV_{DSS}	I_D	I_{DM}	$V_{GS(th)}$ V		at I_D	$R_{DS(on)}$ Ω	at I_D	V_{GS}	P_D	Package
	V	mA	A	Min.	Max.	mA	Max.	mA	V	W	
N-channel											
ZVNL535A	350	90	0.8	0.5	1.5	1	40	50	3	0.7	E-line
ZVNL120A	200	180	2	0.5	1.5	1	10	125	3	0.7	E-line
ZVNL110A	100	320	6	0.75	1.5	1	4.5	250	5	0.7	E-line
ZVN4206A	60	600	8	1.3	3	1	1.5	500	5	0.7	E-line
BSS138	50	200	0.8	0.5	1.5	1	3.5	200	5	0.36	SOT-23
P-channel											
ZVP4105A	-50	-175	-0.52	-0.8	-2.0	-1	10	-100	-5	0.625	E-line
BSS84	-50	-130	-0.52	-0.8	-2.0	-1	10	-100	-5	0.36	SOT-23

TABLE 4: SOT-23 MOSFETS

Part number	BV_{DSS}	I_D	I_{DM}	$V_{GS(th)}$ V		at I_D	$R_{DS(on)}$ Ω	at I_D	V_{GS}	P_D	Package marking
	V	mA	A	Min.	Max.	mA	Max.	mA	V	mW	
N-channel											
ZVN3320F	200	60	1	1.0	3	1	25	100	10	250	MU
BSS123	100	170	0.68	0.8	2.8	1	6	100	10	360	SA
ZVN3310F	100	100	2	0.8	2.4	1	10	500	10	250	MF
ZVN4106F	60	200	3	1.3	3	1	2.5	500	10	250	MZ
2N7002	60	115	0.8	1.0	2.5	0.25	7.5	50	5	200	702
ZVN3306F	60	150	3	0.8	2.4	1	5	500	10	250	MC
VN10LF	60	150	3	0.8	2.5	1	7.5	200	5	250	MY
BS170F	60	150	3	0.8	3	1	5	200	10	250	MV
BSS138	50	200	0.8	0.5	1.5	1	3.5	200	5	360	SS
P-channel											
ZVP1320F	-200	-35	-0.4	-1.5	-3.5	-1	80	-50	-10	250	MT
ZVP3310F	-100	-75	-1.2	-1.5	-3.5	-1	20	-150	-10	250	MR
ZVP3306F	-60	-90	-1.6	-1.5	-3.5	-1	14	-200	-10	250	ML
BSS84	-50	-130	-0.5	-0.8	-2.0	-1	10	-100	-5	360	SP
BS250F	-45	-90	-1.6	-1.5	-3.5	-1	14	-200	-10	250	MX

TABLE 5: QUAD MOSFET ARRAY

Part number	BV_{DSS}	I_D	I_{DM}	$V_{GS(th)}$ V		at I_D	$R_{DS(on)}$ Ω	at I_D	V_{GS}	P_D	Package
	V	mA	A	Min.	Max.	mA	Max.	mA	V	W	
N-channel											
ZVN2110E	100	320	3	0.8	2.4	1	4	1000	10	0.85	Plastic DIL
ZVN4206E	60	600	3	1.3	3.0	1	1.5	500	5	0.85	Plastic DIL
ZVN2106E	60	450	3	0.8	2.4	1	2	1000	10	0.85	Plastic DIL
ZVN3306E	60	270	3	0.8	2.4	1	5	500	10	0.85	Plastic DIL
P-channel											
ZVP2110E	-100	-230	-3	-1.5	-3.5	-1	8	-375	-10	0.85	Plastic DIL
ZVP2106E	-60	-280	-3	-1.5	-3.5	-1	5	-500	-10	0.85	Plastic DIL
ZVP3306E	-60	-160	-1.6	-1.5	-3.5	-1	14	-200	-10	0.85	Plastic DIL

SELECTION TABLES

TABLE 6: CENTRE DRAIN CONFIGURATION E-LINE MOSFETS

Part number	BV_{DSS}	I_D	I_{DM}	$V_{GS(th)}$			$R_{DS(on)}$			P_D	Package
	V	mA	A	V Min.	Max.	at I_D mA	Ω Max.	at I_D mA	V_{GS} V	W	
N-channel											
ZVN2120C	200	180	2	1	3	1	10	250	10	0.7	E-line
ZVN2110C	100	320	6	0.8	2.4	1	4	1000	10	0.7	E-line
ZVN4206C	60	600	8	1.3	3	1	1.5	500	5	0.7	E-line
N-channel low threshold											
ZVNL120C	200	180	2	0.5	1.5	1	10	125	3	0.7	E-line
P-channel											
ZVP2120C	−200	−120	−1.2	−1.5	−3.5	−1	25	−150	−10	0.7	E-line
ZVP2110C	−100	−230	−3	−1.5	−3.5	−1	8	−375	−10	0.7	E-line
ZVP2106C	−60	−280	−4	−1.5	−3.5	−1	5	−500	−10	0.7	E-line

TABLE 7: SOT-223 MOSFETS

Part number	BV_{DSS}	I_D	I_{DM}	P_{tot}	$V_{GS(th)}$			$R_{DS(on)}$			Complement
	V	A	A	W	V Min.	Max.	at I_D mA	Ω Max.	at I_D A	V_{GS} V	
N-channel											
ZVN2106G	60	0.7	8	2	0.8	2.4	1.0	2.0	1.0	10	ZVP2106G
P-channel											
ZVP2106G	−60	−0.45	−4	2	−1.5	−3.5	−1.0	5.0	−0.5	−10	ZVN2106G

APPROVALS

TABLE 9 : ZETEX PART NUMBER/BS-CECC CROSS REFERENCE

Part number	BS-CECC No.
ZVN0535A	50012-019
ZVN0540A	50012-019
ZVN0545A	50012-019
ZVN2106A	50012-018
ZVN2106B	50012-031
ZVN2110A	50012-018

Part number	BS-CECC No.
ZVN2110B	50012-031
ZVP2106A	50012-033
ZVP2106B	50012-034
ZVP2110A	50012-033
ZVP2110B	50012-034

TABLE 10 : BS-CECC/ZETEX PART NUMBER CROSS REFERENCE

BS-CECC No.	Part number
50012-018	ZVN2106A ZVN2110A
50012-019	ZVN0535A ZVN0540A ZVN0545A
50012-031	ZVN2106B ZVN2110B

BS-CECC No.	Part number
50012-033	ZVP2106A ZVP2110A
50012-034	ZVP2106B ZVP2110B

ORDERING INFORMATION

When ordering BS-CECC approved products the following prefix/suffix apply.

EXAMPLES:

E-Line devices (prefix BSI)
BSIZVN2110A to BS-CECC 50012-018

TO-39 devices (suffix BS)
ZVN2110BBS to BS-CECC 50012-031

DEVICE RATINGS, SPECIFICATIONS AND CHARACTERISTICS

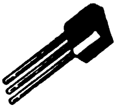
This section contains the range of MOSFET's offered by Zetex. Some changes to earlier published data have been made. The data presented here supersedes all previous specifications.

N-channel enhancement mode vertical DMOS FET

2N7000

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)

DESCRIPTION

A compact cell geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
2N7000	60V	0.2A	5Ω

2N7000

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	Unit
V_{DS}	Drain-source voltage	60	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.2	A
I_{DM}	Pulse drain current	0.5	A
V_{GS}	Gate-source voltage	±40	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.4	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25°C$ unless otherwise stated).

Parameter		Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	60	—	V	$I_D = 10\mu A$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	0.8	3	V	$I_D = 1\,mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	—	10	nA	$V_{GS} = \pm 15V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	—	1	μA	$V_{DS} = 48V$, $V_{GS} = 0V$
		—	1	mA	$V_{DS} = 48V$, $V_{GS} = 0V$ ($T = 125°C$) (2)
$I_{D(on)}$	On-state drain current (1)	75	—	mA	$V_{DS} = 10V$, $V_{GS} = 4.5V$
$V_{DS(on)}$	Static drain-source on-state voltage (1)	—	2.5	V	$V_{GS} = 10V$, $I_D = 500mA$
		—	0.4	V	$V_{GS} = 4.5V$, $I_D = 75mA$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	—	5	Ω	$I_D = 500mA$, $V_{GS} = 10V$
g_{fs}	Forward transconductance (1) (2)	100	—	mS	$V_{DS} = 10V$, $I_D = 200mA$
C_{iss}	Input capacitance (2)	—	60	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ $f = 1\,MHz$
C_{oss}	Common source output capacitance	—	25	pF	
C_{rss}	Reverse transfer capacitance (2)	—	5	pF	
$t_{(on)}$	Turn-on time (2)	—	10	ns	$V_{DD} \approx 15V$, $I_D = 500mA$ $R_g = 25\Omega$, $R_L = 25\Omega$
$t_{(off)}$	Turn-off time (2)	—	10	ns	

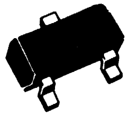
Notes (1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.
(2) Sample test.

N-channel enhancement mode vertical DMOS FET

2N7002

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



SOT-23

DESCRIPTION

A compact cell geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
2N7002	60V	115mA	7.5Ω

2N7002

ABSOLUTE MAXIMUM RATINGS

Parameters		SOT-23	Unit
V_{DS}	Drain-source voltage	60	V
I_D	Continuous drain current (@ $T_A = 25°C$)	115	mA
I_{DM}	Pulsed drain current	800	mA
V_{GS}	Gate-source voltage	±40	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	200	mW
T_j, T_{stg}	Operating/storage temperature range	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25°C$ unless otherwise stated).

Parameter		Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	60	–	V	$I_D = 10\mu A$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	1.0	2.5	V	$I_D = 250\mu A$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	1	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	500	μA	V_{DS} = Max. rating, $V_{GS} = 0V$ ($T = 125°C$) (2)
$I_{D(on)}$	On-state drain current (1)	500	–	mA	$V_{DS} = 25V$, $V_{GS} = 10V$
$V_{DS(on)}$	Static drain-source on-state voltage (1)	–	3.75	V	$V_{GS} = 10V$, $I_D = 500mA$
		–	0.375	V	$V_{GS} = 5V$, $I_D = 50mA$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	7.5	Ω	$I_D = 500mA$, $V_{GS} = 10V$
		–	7.5	Ω	$I_D = 50mA$, $V_{GS} = 5V$
g_{fs}	Forward transconductance (1) (2)	80	–	mS	$V_{DS} = 25V$, $I_D = 500mA$
C_{iss}	Input capacitance (2)	–	50	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ $f = 1 MHz$
C_{oss}	Common source output capacitance (2)	–	25	pF	
C_{rss}	Reverse transfer capacitance (2)	–	5	pF	
$t_{(on)}$	Turn-on time (2)	–	20	ns	$V_{DD} \approx 30V$, $I_D = 200mA$ $R_g = 25\Omega$, $R_L = 150\Omega$
$t_{(off)}$	Turn-off time (2)	–	20	ns	

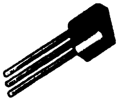
Notes (1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.
(2) Sample test.

N-channel enhancement mode vertical DMOS FET

BS107P

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)

DESCRIPTION

A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
BS107P	200V	0.12A	23Ω

BS107P

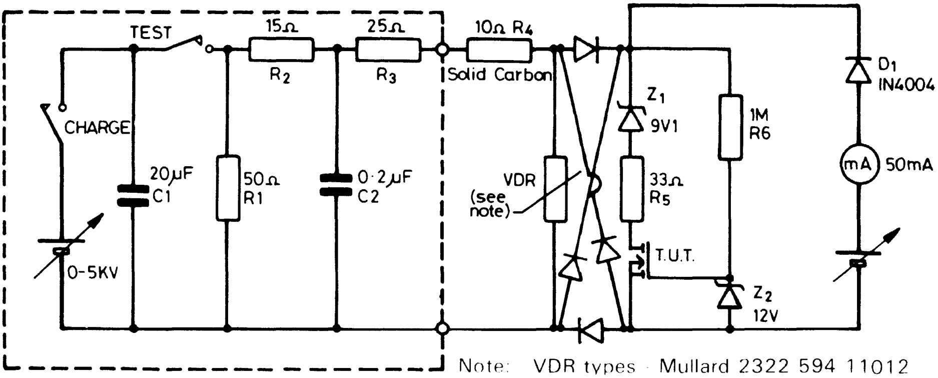
ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	Unit
V_{DS}	Drain-source voltage	200	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.12	A
I_{DM}	Pulsed drain current	2	A
V_{GS}	Gate-source voltage	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.5	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Typ.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	200	230	–	V	$I_D = 100\mu A$, $V_{GS} = 0V$
I_{GSS}	Gate body leakage	–	–	10	nA	$V_{GS} = 15V$, $V_{DS} = 0V$
I_{DSS}	Drain cut-off current	–	–	30	nA	$V_{DS} = 130V$, $V_{GS} = 0V$
I_{DSX}		–	–	1	μA	$V_{DS} = 70V$, $V_{GS} = 0.2V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	15	28	Ω	$I_D = 20mA$, $V_{GS} = 2.6V$
		–	–	30	Ω	$I_D = 100mA$, $V_{GS} = 2.7V$

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.



Note: VDR types Mullard 2322 594 11012
Siemens S10V S07K 75
Matsushita ER2-C070K 10

The transistor under test should withstand a surge applied via above circuit when C1 is charged to 1.5kV.

Fig. 1 Surge test circuit

6872

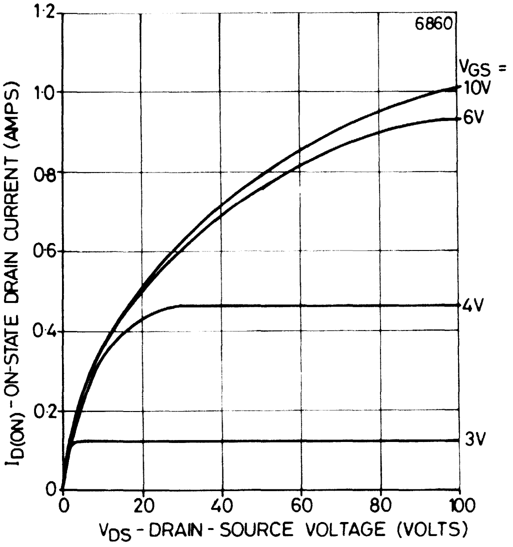


Fig. 2 Typical output characteristics

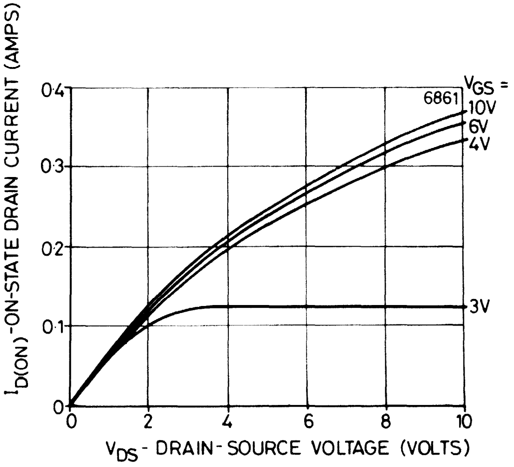


Fig. 3 Typical saturation characteristics

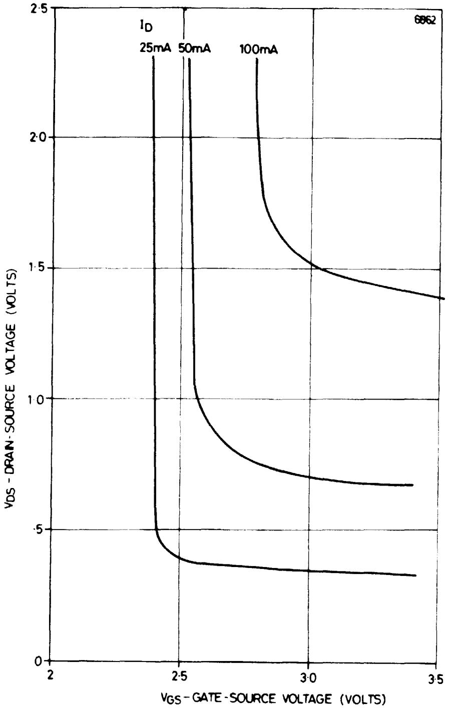


Fig. 4 Typical voltage saturation characteristics

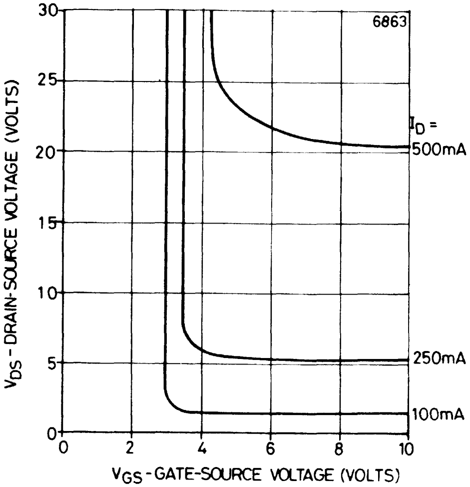


Fig. 5 Typical voltage saturation characteristics

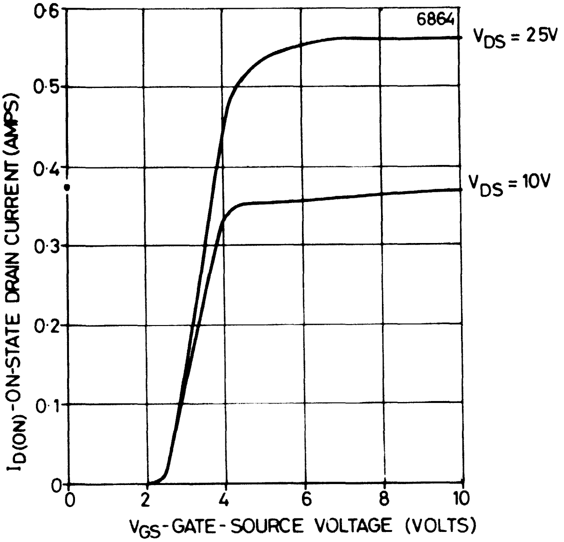


Fig. 6 Typical transfer characteristics

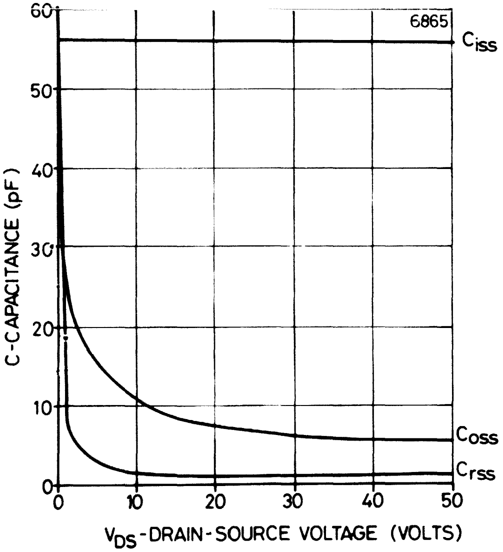


Fig. 7 Typical capacitance v drain-source voltage

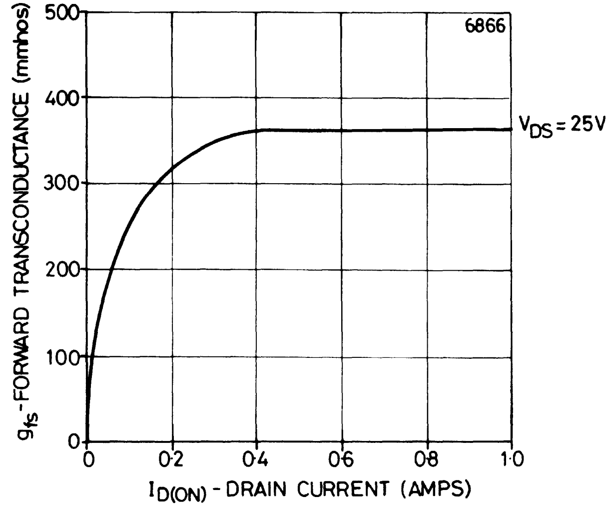


Fig. 8 Typical transconductance v drain current

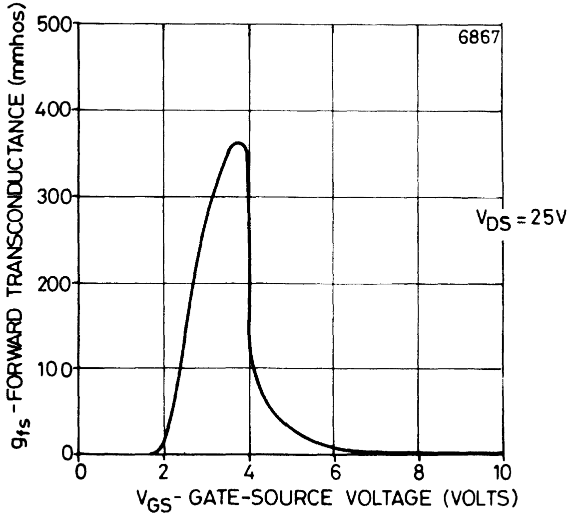


Fig. 9 Typical transconductance v gate-source voltage

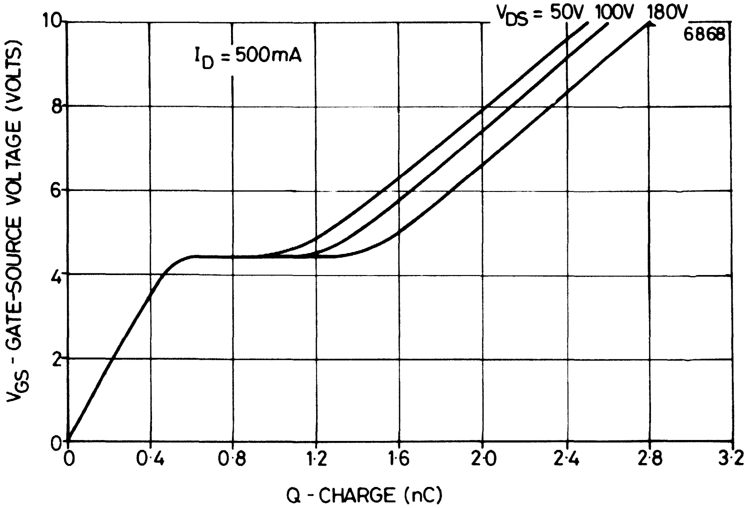


Fig. 10 Typical gate charge v gate-source voltage

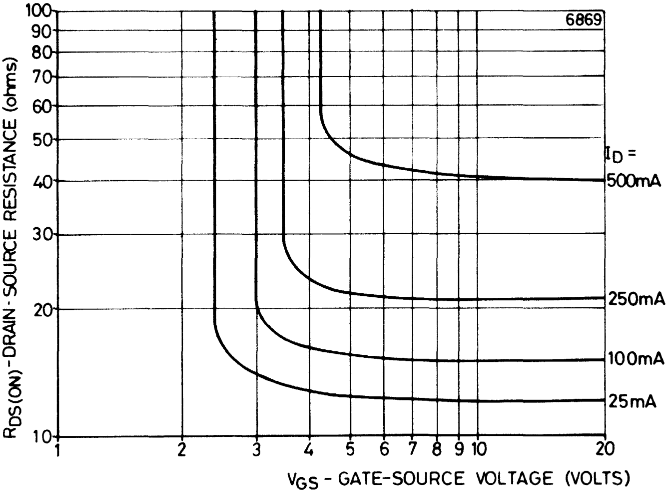


Fig. 11 Typical on-resistance v gate-source voltage

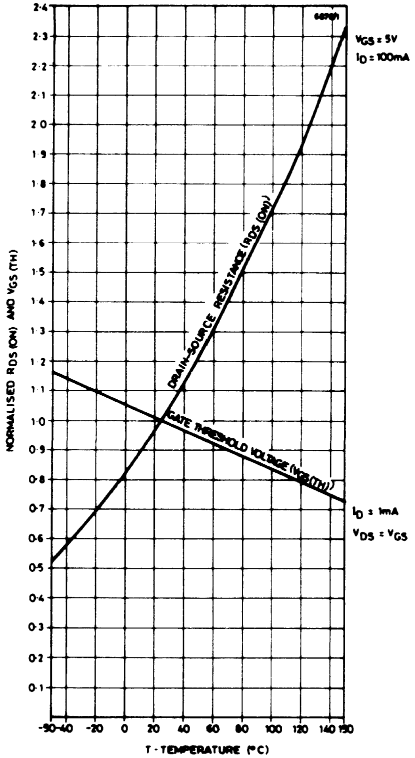


Fig. 12 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

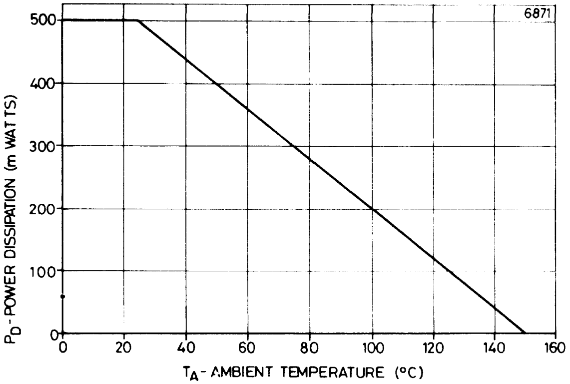


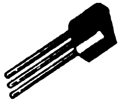
Fig. 13 Power v temperature derating curve (ambient)

N-channel enhancement mode vertical DMOS FET

BS107PT

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)

DESCRIPTION

A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
BS107PT	200V	0.12A	28Ω

BS107PT

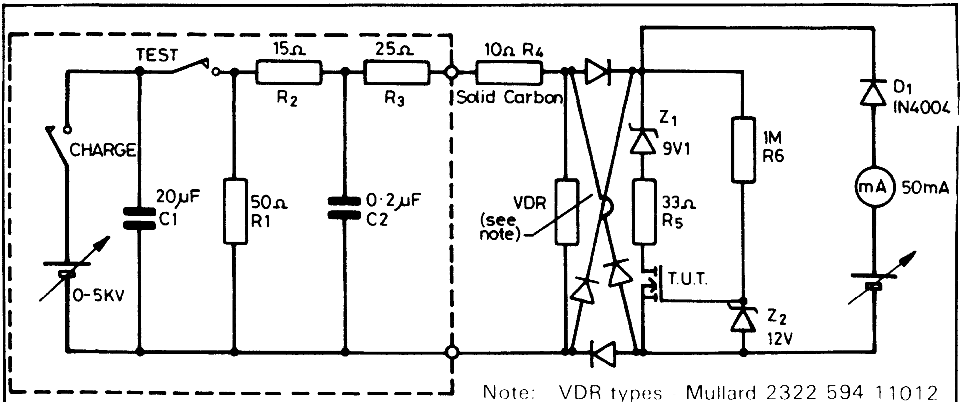
ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	Unit
V_{DS}	Drain-source voltage	200	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.12	A
I_{DM}	Pulsed drain current	2	A
V_{GS}	Gate-source voltage	± 20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.5	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Typ.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	200	230	–	V	$I_D = 100\mu A$, $V_{GS} = 0V$
I_{GSS}	Gate body leakage	–	–	10	nA	$V_{GS} = 15V$, $V_{DS} = 0V$
I_{DSS}	Drain cut-off current	–	–	30	nA	$V_{DS} = 130V$, $V_{GS} = 0V$
I_{DSX}		–	–	1	µA	$V_{DS} = 70V$, $V_{GS} = 0.2V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	15	28	Ω	$I_D = 20mA$, $V_{GS} = 2.6V$
		–	–	30	Ω	$I_D = 100mA$, $V_{GS} = 2.7V$

(1) Measured under pulsed conditions. Width = 300µs. Duty cycle ⩽ 2%.



Note: VDR types Mullard 2322 594 11012
Siemens S10V S07K 75
Matsushita ER2 C070K 10

The transistor under test should withstand a surge applied via above circuit when C1 is charged to 1.5kV.

Fig. 1 Surge test circuit

6872

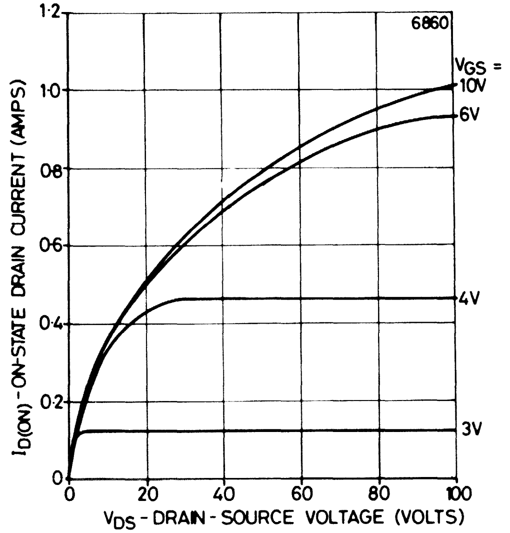


Fig. 2 Typical output characteristics

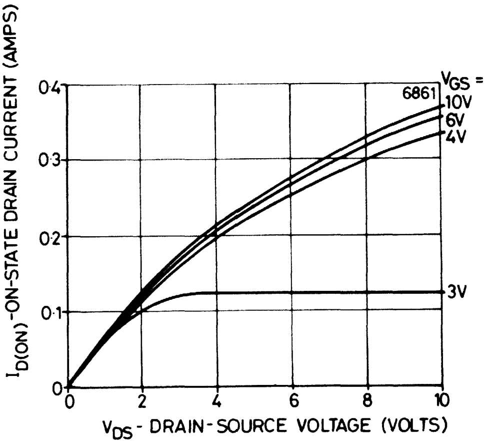


Fig. 3 Typical saturation characteristics

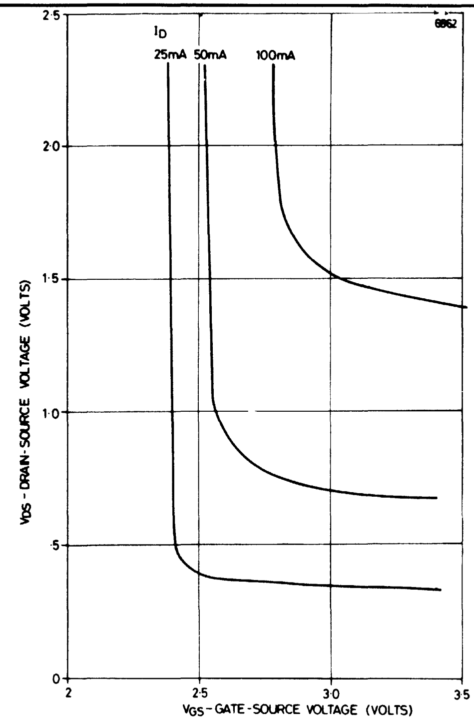


Fig. 4 Typical voltage saturation characteristics

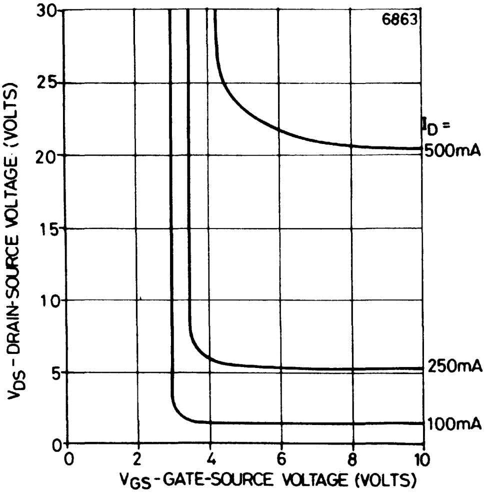


Fig. 5 Typical voltage saturation characteristics

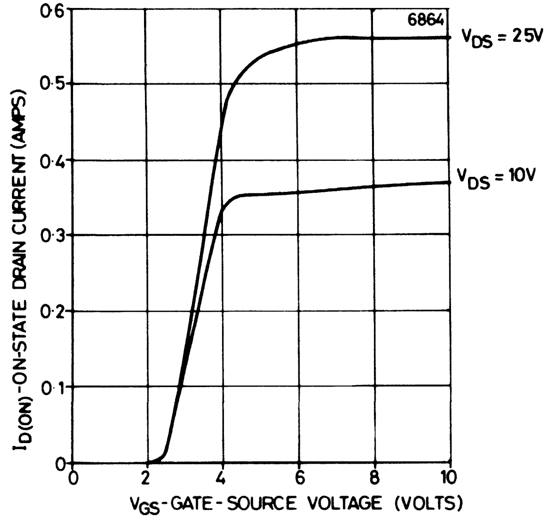


Fig. 6 Typical transfer characteristics

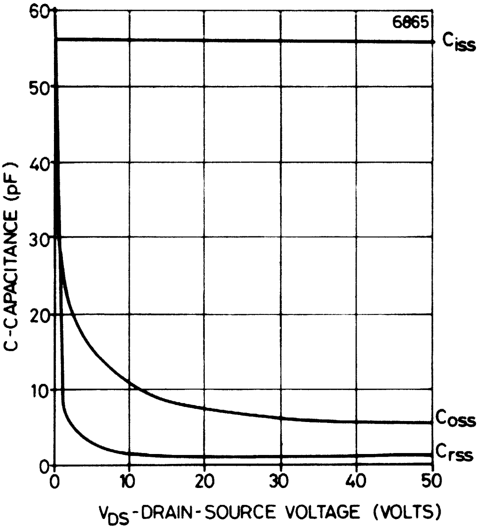


Fig. 7 Typical capacitance v drain-source voltage

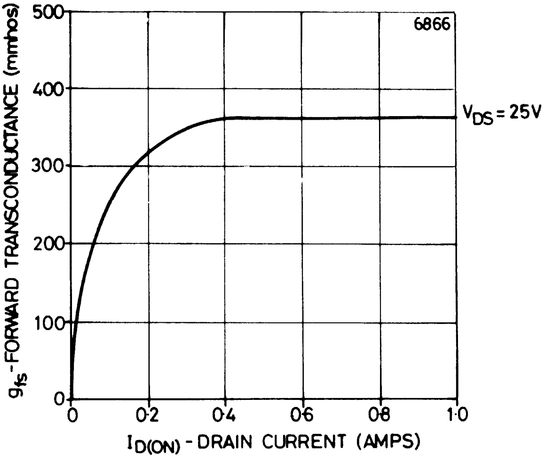


Fig. 8 Typical transconductance v drain current

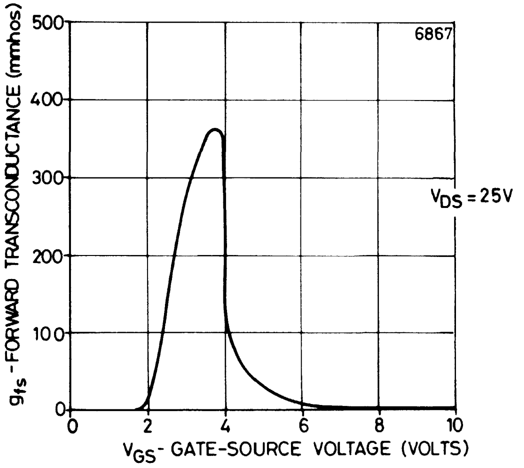


Fig. 9 Typical transconductance v gate-source voltage

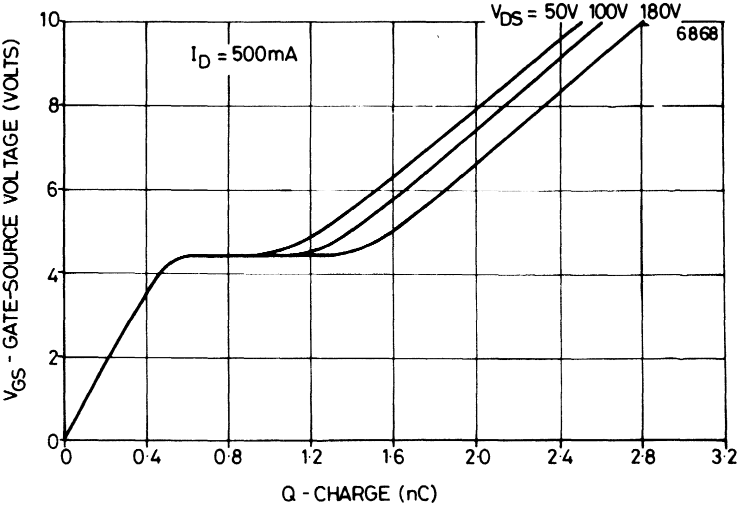


Fig. 10 Typical gate charge v gate-source voltage

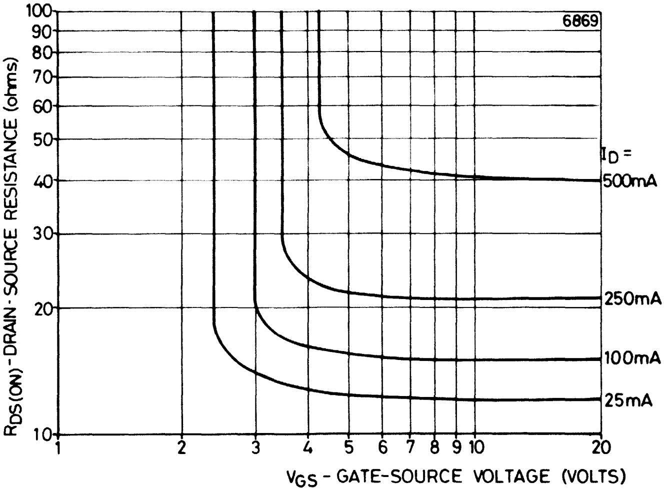


Fig. 11 Typical on-resistance v gate-source voltage

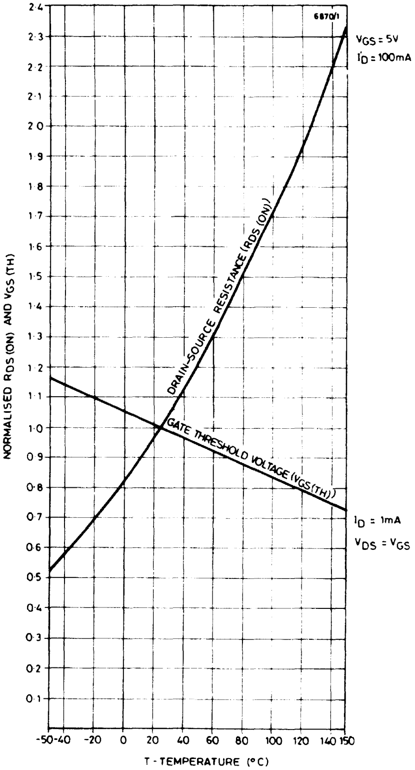


Fig. 12 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

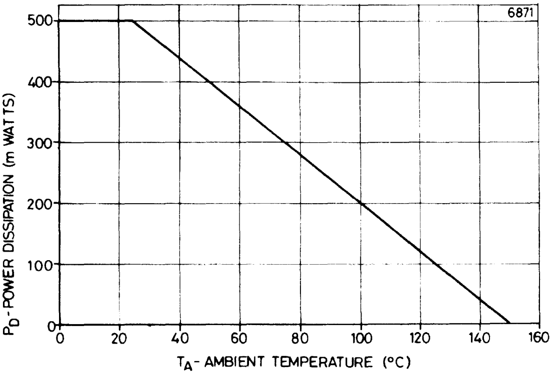


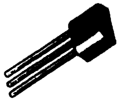
Fig. 13 Power v temperature derating curve (ambient)

N-channel enhancement mode vertical DMOS FET

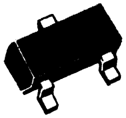
BS170

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)
SUFFIX P



SOT-23
SUFFIX F

DESCRIPTION

A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
BS170P	60V	0.27A	5Ω
BS170F	60V	0.15A	5Ω

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	SOT-23	Units
V_{DS}	Drain-source voltage	60	60	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.27	0.15	A
I_{DM}	Pulsed drain current	3	3	A
V_{GS}	Gate-source voltage	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.625	0.25	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Typ.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	60	90	–	V	$I_D = 100\mu A$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	0.8	–	3	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	–	10	nA	$V_{GS} = 15V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	–	0.5	μA	$V_{DS} = 25V$, $V_{GS} = 0V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	–	5	Ω	$I_D = 200mA$, $V_{GS} = 10V$
g_{fs}	Forward transconductance (1) (2)	–	200	–	mS	$V_{DS} = 10V$, $I_D = 200mA$
C_{iss}	Input capacitance (2)	–	60	–	pF	$V_{DS} = 10V$, $V_{GS} = 0V$ f = 1MHz
$t_{(on)}$	Turn-on time (2) (3)	–	–	10	ns	$V_{DD} \approx 15V$, $I_D = 600mA$
$t_{(off)}$	Turn-off time (2) (3)	–	–	10	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽2%.

(2) Sample test.

(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

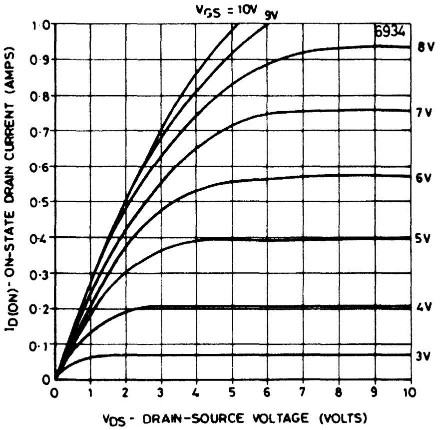


Fig. 1 Typical saturation characteristics

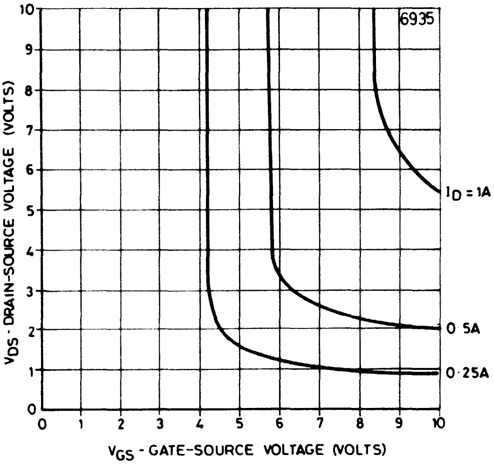


Fig. 2 Typical voltage saturation characteristics

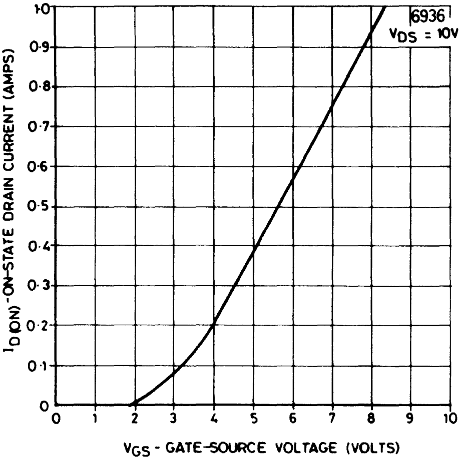


Fig. 3 Typical transfer characteristics

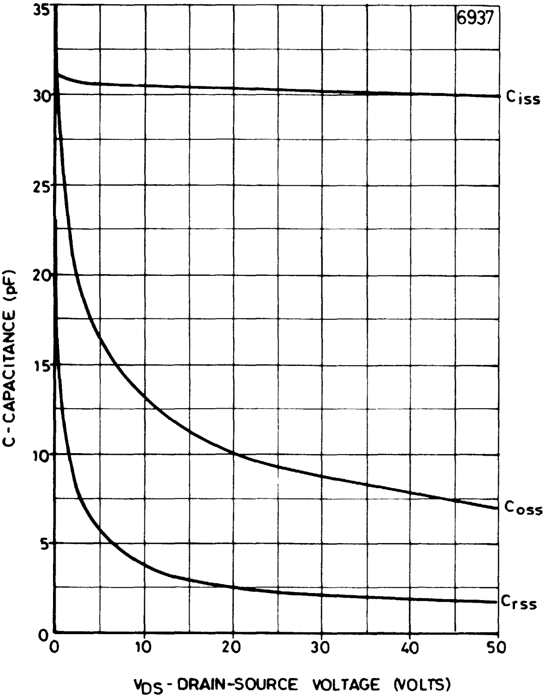


Fig. 4 Typical capacitance v drain-source voltage

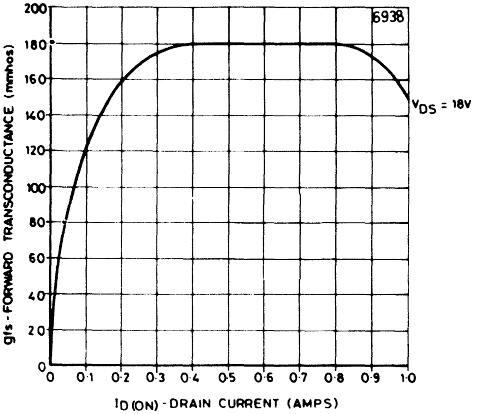


Fig. 5 Typical transconductance v drain current

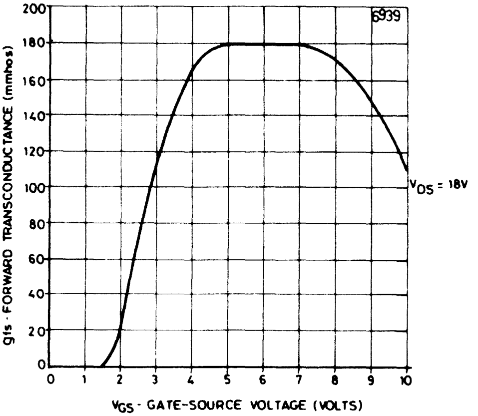


Fig. 6 Typical transconductance v gate-source voltage

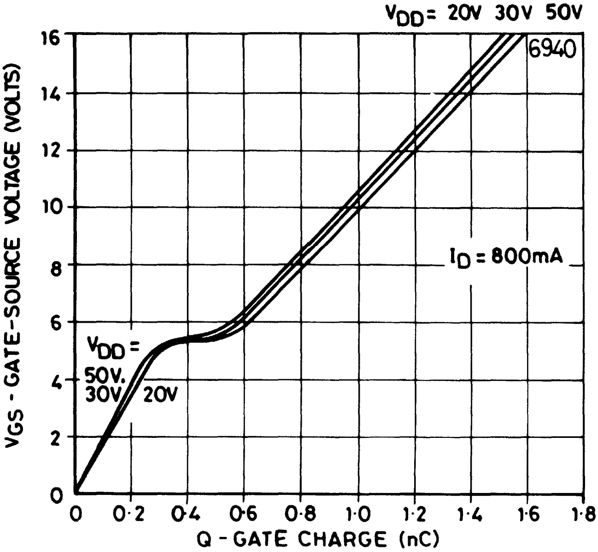


Fig. 7 Typical gate charge v gate-source voltage

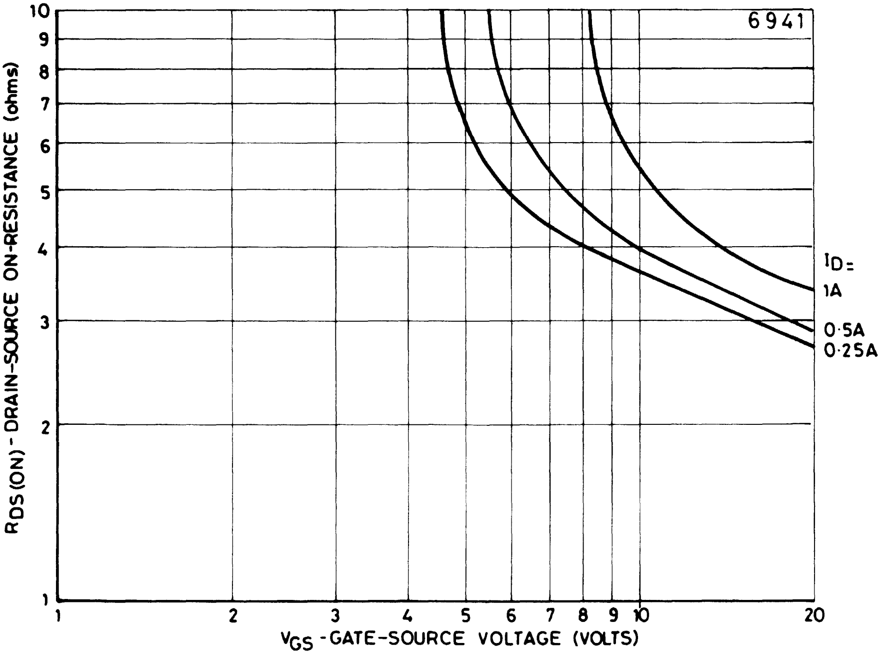


Fig. 8 Typical on-resistance v gate-source voltage

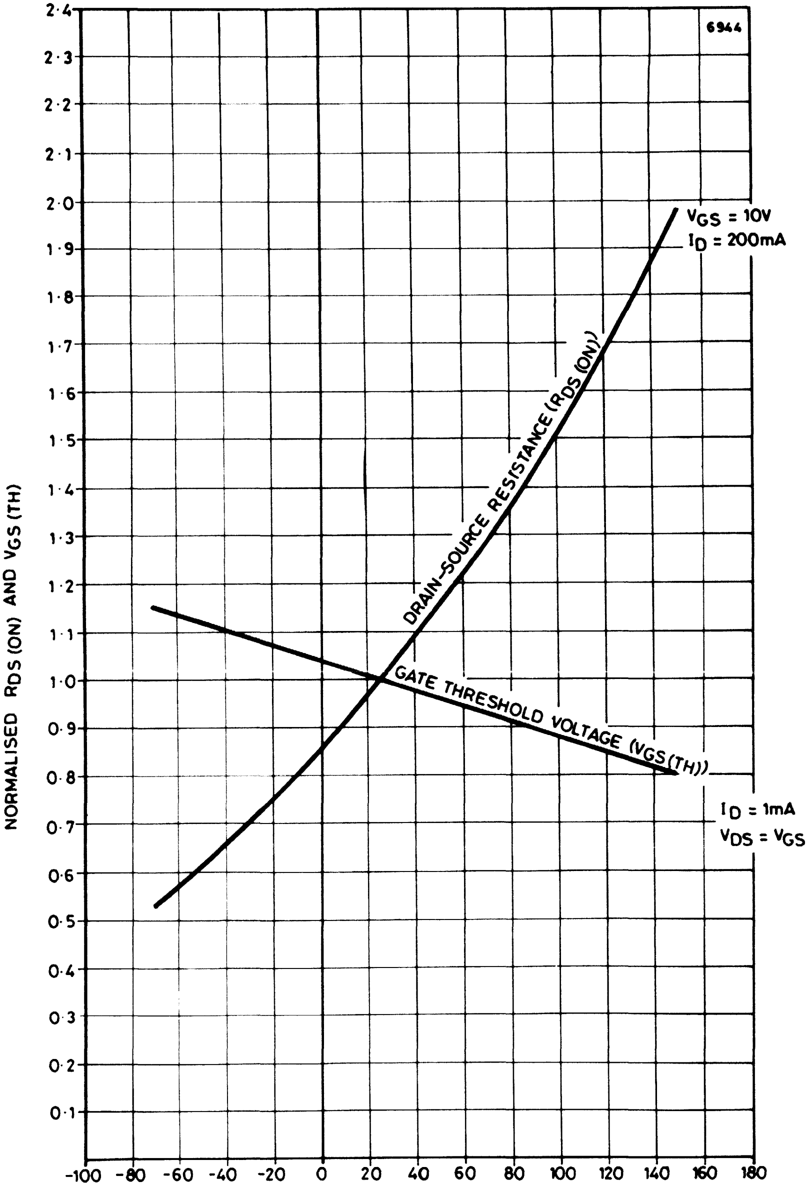


Fig. 9 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

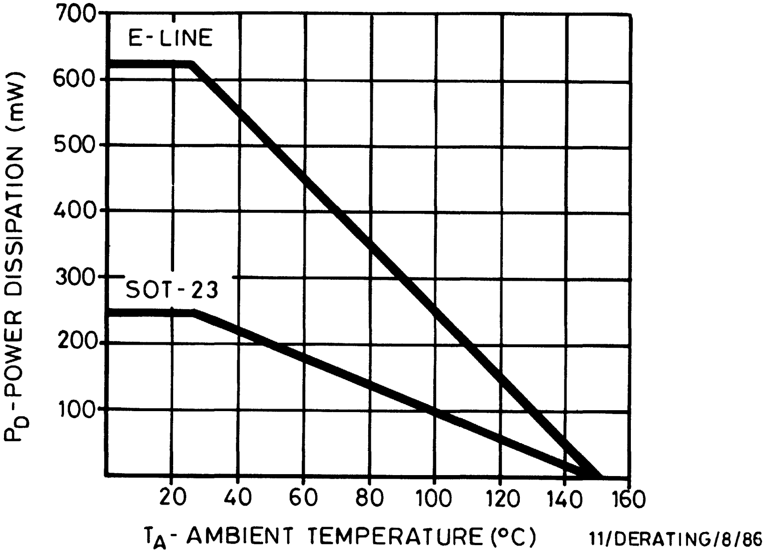


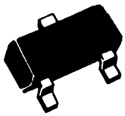
Fig. 10 Power v temperature derating curve (ambient)

P-channel enhancement mode vertical DMOS FET

BS250F

FEATURES

- **Compact geometry**
- **Fast switching speeds**
- **No secondary breakdown**
- **Excellent temperature stability**
- **High input impedance**
- **Low current drive**
- **Ease of paralleling**



SOT-23

DESCRIPTION

A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
BS250F	−45V	−0.9A	14Ω

BS250F

ABSOLUTE MAXIMUM RATINGS

Parameters		SOT-23	Unit
V_{DS}	Drain-source voltage	−45	V
I_D	Continuous drain current (@ $T_A = 25°C$)	−0.09	A
I_{DM}	Pulsed drain current	−1.6	A
V_{GS}	Gate-source voltage	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.25	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Typ.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	−45	−70	–	V	$I_D = -100\mu A$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	−1	–	−3.5	V	$I_D = -1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	–	−20	nA	$V_{GS} = -15V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	–	−0.5	μA	$V_{DS} = -25V$, $V_{GS} = 0V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	9	14	Ω	$I_D = -200mA$, $V_{GS} = -10V$
g_{fs}	Forward transconductance (1) (2)	–	90	–	mS	$V_{DS} = -10V$, $I_D = -200mA$
C_{iss}	Input capacitance (2)	–	25	–	pF	$V_{DS} = -10V$, $V_{GS} = 0V$ f = 1MHz
$t_{d(on)}$	Turn-on delay time (2) (3)	–	–	10	ns	$V_{DD} \approx -25V$, $I_D = -200mA$
t_r	Rise time (2) (3)	–	–	10	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	–	10	ns	
t_f	Fall time (2) (3)	–	–	10	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽2%.

(2) Sample test.

(3) Switching times measured with 50Ω source impedance and <5ns rise time on a pulse generator.

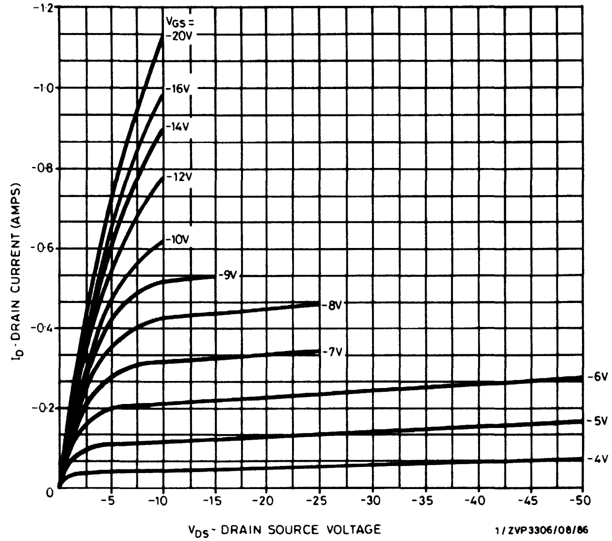


Fig. 1 Typical output characteristics

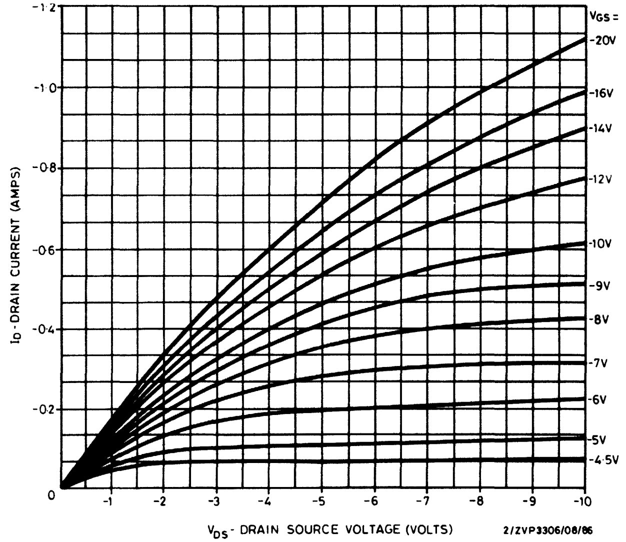


Fig. 2 Typical saturation characteristics

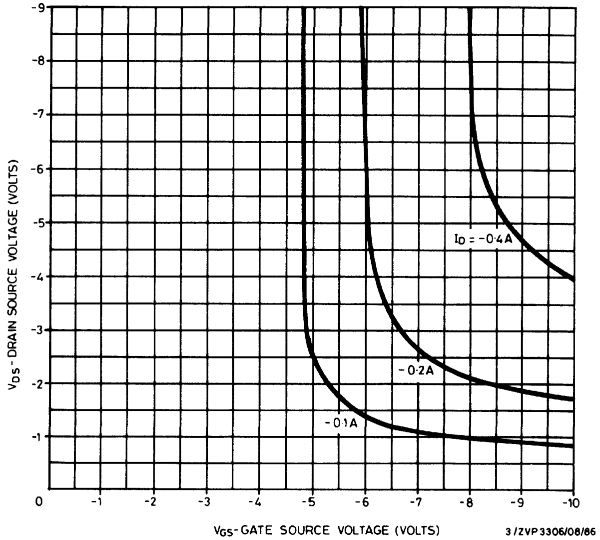


Fig. 3 Typical voltage saturation characteristics

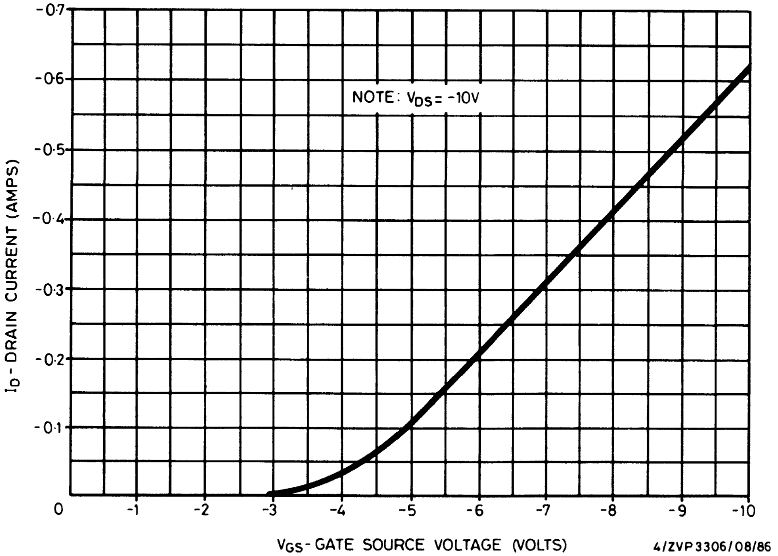


Fig. 4 Typical transfer characteristics

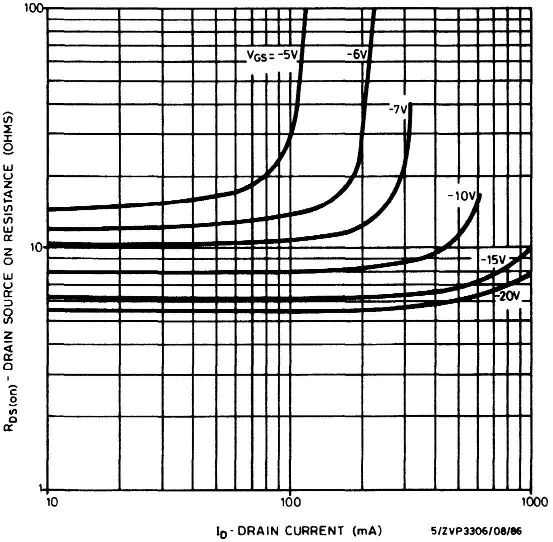


Fig. 5 Typical on-resistance v drain current

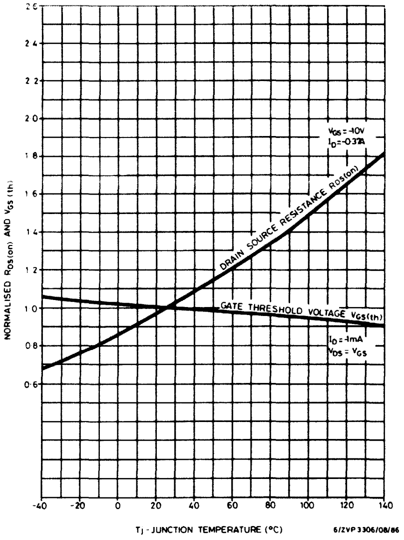


Fig. 6 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

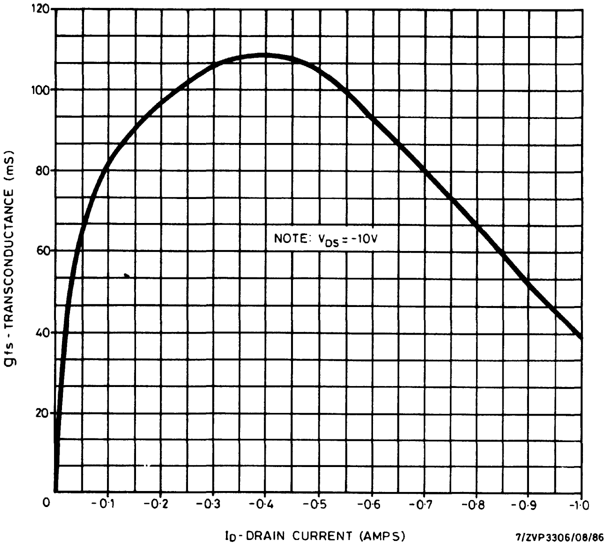


Fig. 7 Typical transconductance v drain current

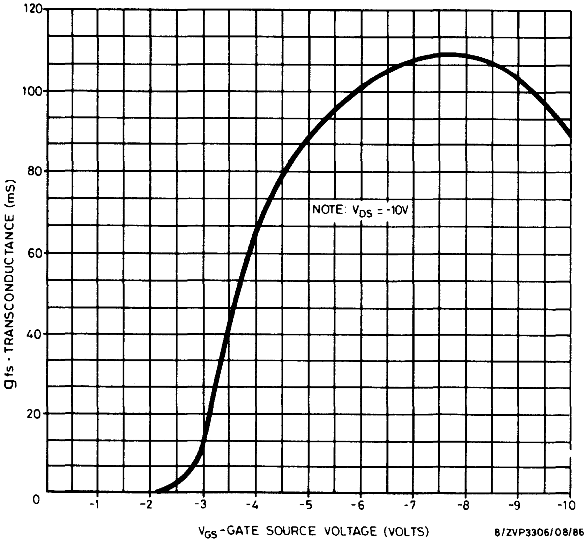


Fig. 8 Typical transconductance v gate-source voltage

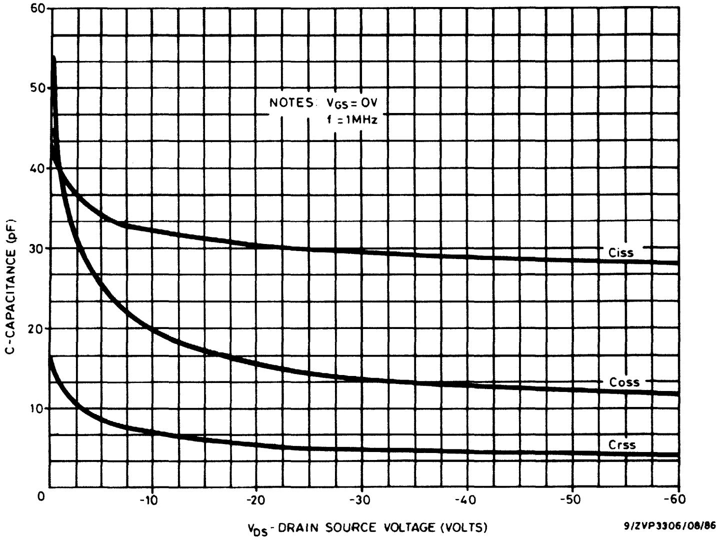


Fig. 9 Typical capacitance v drain-source voltage

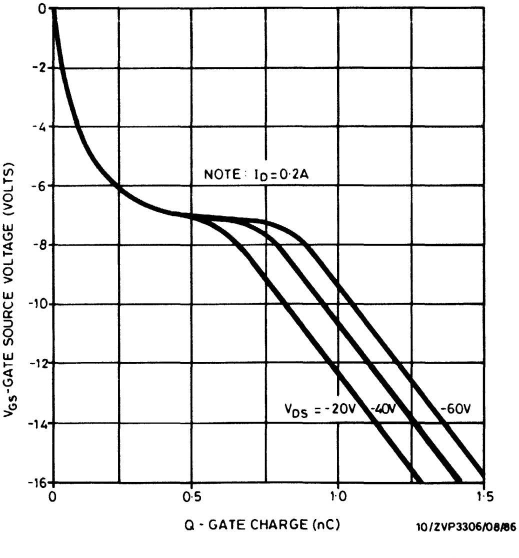


Fig. 10 Typical gate charge v gate-source voltage

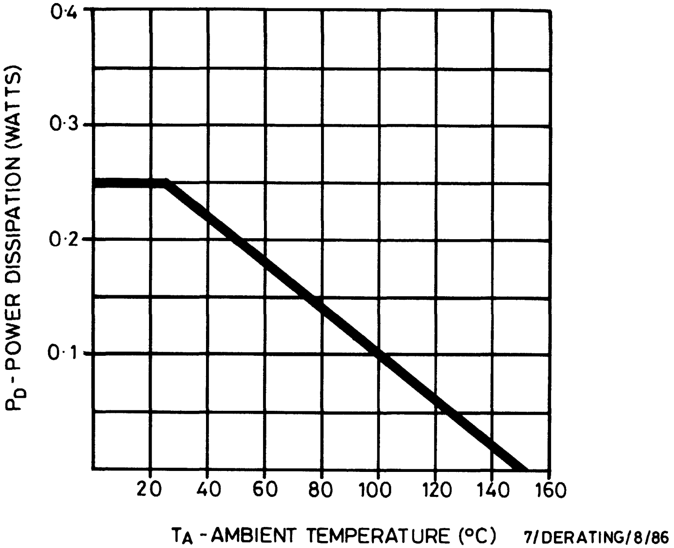


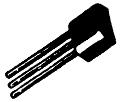
Fig. 11 Power v temperature derating curve (ambient)

P-channel enhancement mode vertical DMOS FET

BS250P

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)

DESCRIPTION

A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
BS250P	−45V	−0.23A	14Ω

BS250P

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	Unit
V_{DS}	Drain-source voltage	−45	V
I_D	Continuous drain current (@ $T_A = 25°C$)	−0.23	A
I_{DM}	Pulsed drain current	−3	A
V_{GS}	Gate-source voltage	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Typ.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	−45	−70	–	V	$I_D = -100\mu A$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	−1	–	−3.5	V	$I_D = -1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	–	−20	nA	$V_{GS} = -15V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	–	−0.5	μA	$V_{DS} = -25V$, $V_{GS} = 0V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	–	14	Ω	$I_D = -200mA$, $V_{GS} = -10V$
g_{fs}	Forward transconductance (1) (2)	–	150	–	mS	$V_{DS} = -10V$, $I_D = -200mA$
C_{iss}	Input capacitance (2)	–	60	–	pF	$V_{DS} = -10V$, $V_{GS} = 0V$ f = 1MHz
$t_{d(on)}$	Turn-on delay time (2) (3)	–	–	10	ns	$V_{DD} \approx -25V$, $I_D = -500mA$
t_r	Rise time (2) (3)	–	–	10	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	–	10	ns	
t_f	Fall time (2) (3)	–	–	10	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ≤ 2%.

(2) Sample test.

(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

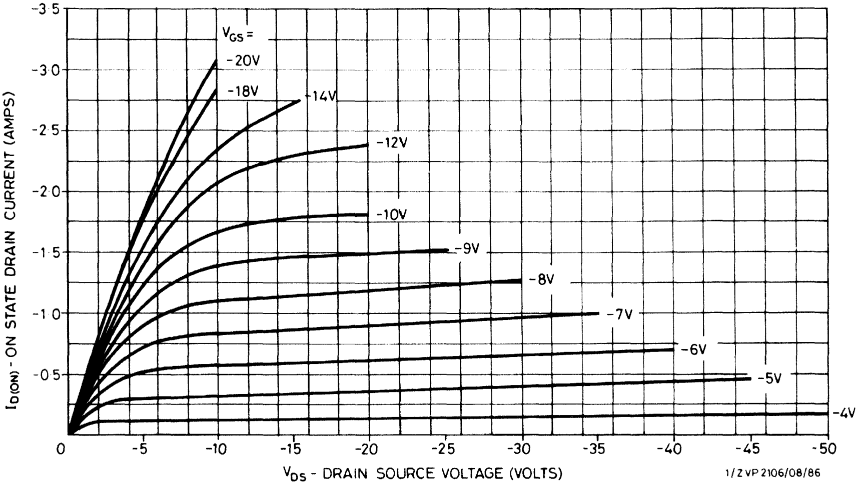


Fig. 1 Typical output characteristics

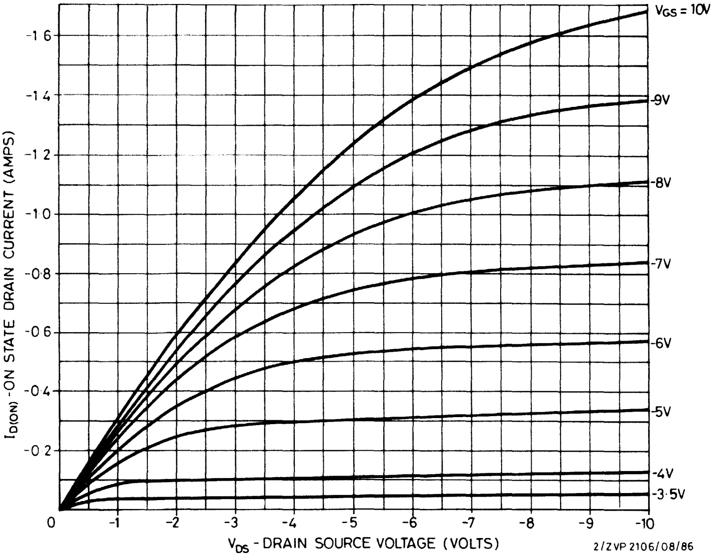


Fig. 2 Typical saturation characteristics

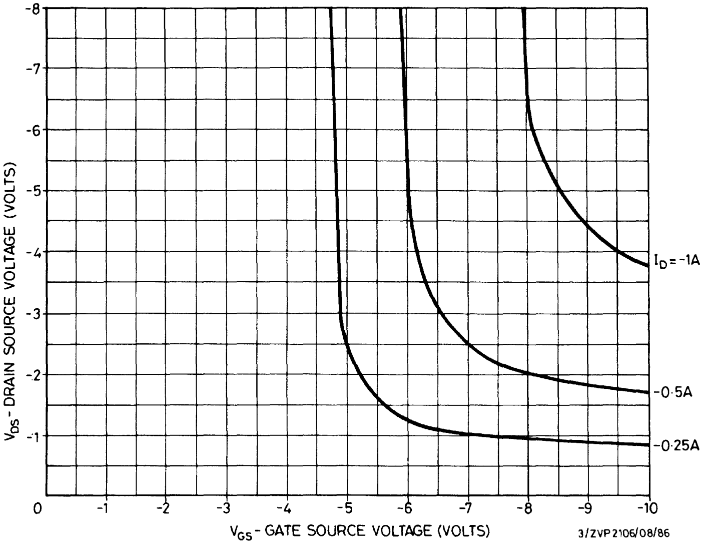


Fig. 3 Typical voltage saturation characteristics

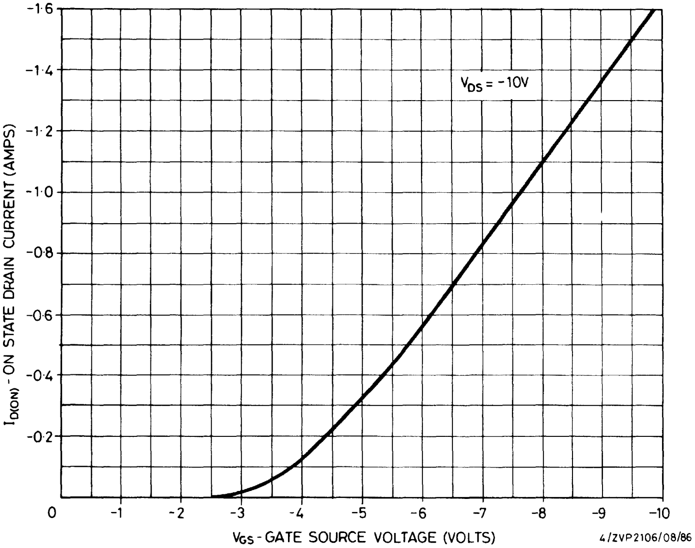


Fig. 4 Typical transfer characteristics

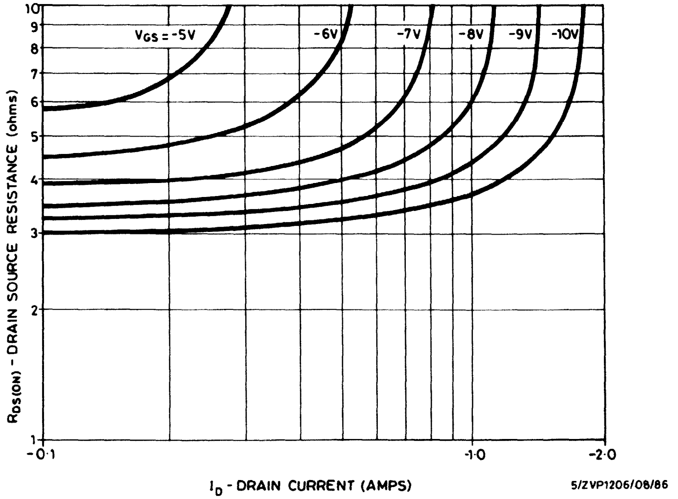


Fig. 5 Typical on-resistance v drain current

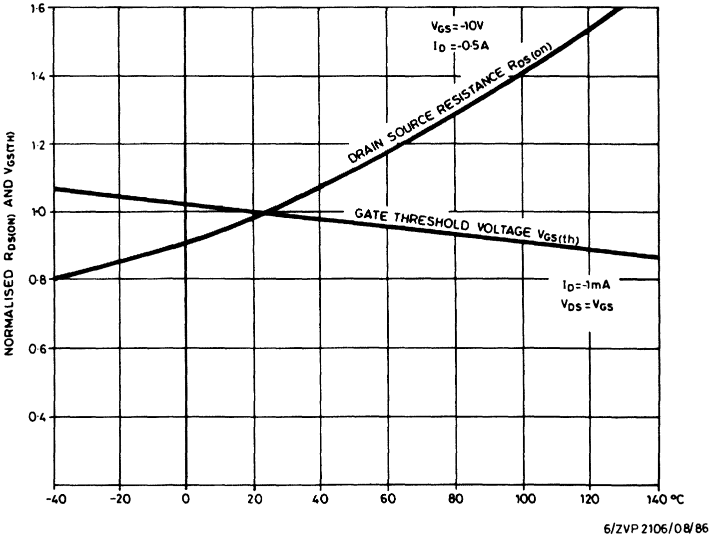


Fig. 6 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

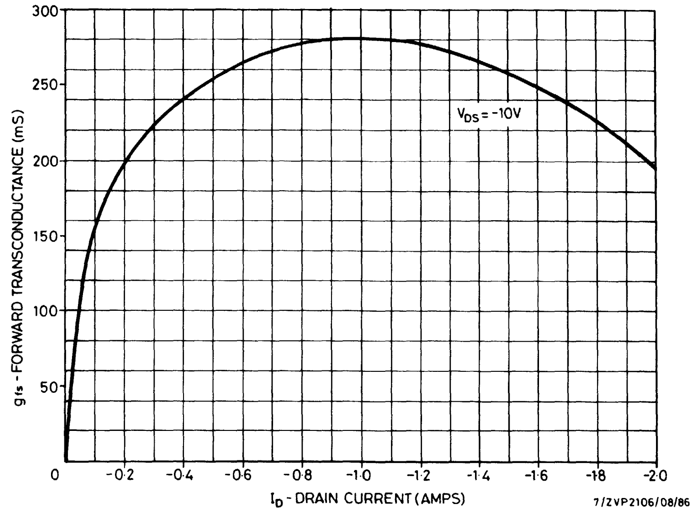


Fig. 7 Typical transconductance v drain current

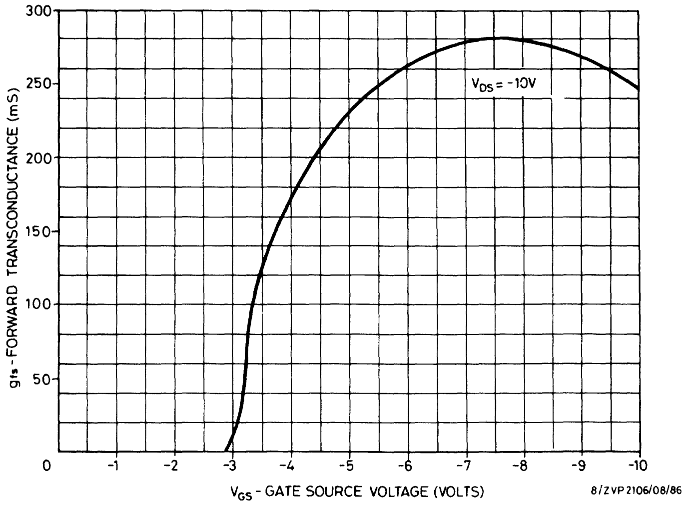


Fig. 8 Typical transconductance v gate-source voltage

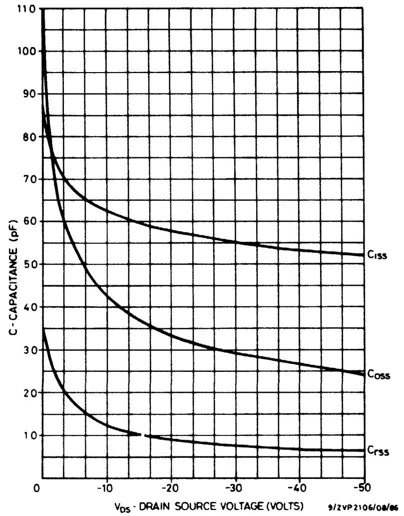


Fig. 9 Typical capacitance v drain-source voltage

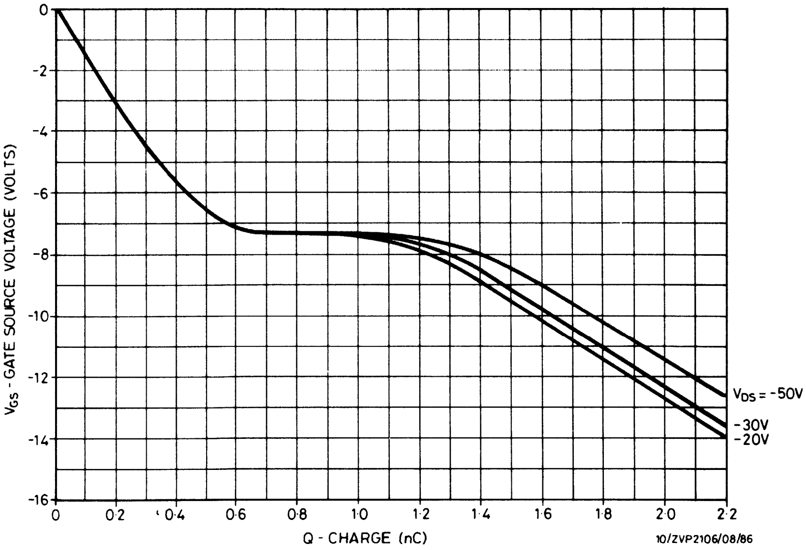


Fig. 10 Typical gate charge v gate-source voltage

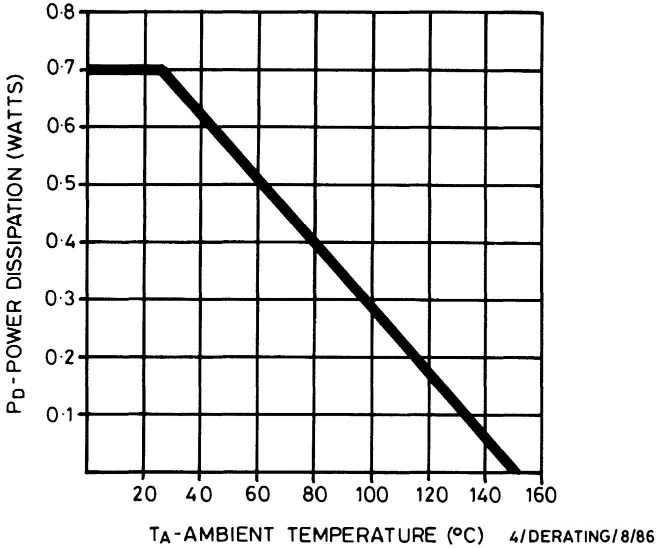


Fig. 11 Power v temperature derating curve (ambient)

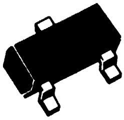
P-channel enhancement mode vertical DMOS FET

PROVISIONAL DATA

BSS84

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



SOT-23

DESCRIPTION

A compact cell geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
BSS84	−50V	−130mA	10Ω

BSS84

ABSOLUTE MAXIMUM RATINGS

	Parameters	SOT-23	Unit
V_{DS}	Drain-source voltage	−50	V
I_D	Continuous drain current (@ $T_A = 25°C$)	−130	mA
I_{DM}	Pulsed drain current	−520	mA
V_{GS}	Gate-source voltage	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.36	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25°C$ unless otherwise stated).

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-source breakdown voltage	BV_{DSS}	−50	—	—	V	$V_{GS} = 0V$ $I_D = -0.25mA$
Gate-source threshold voltage	$V_{GS(th)}$	−0.8	−1.5	−2.0	V	$V_{DS} = V_{GS}$ $I_D = -1mA$
Zero gate voltage drain current	I_{DSS}	—	−1	−15	μA	$T_j = 25°C$
		—	−2	−60	μA	$T_j = 125°C$ $V_{DS} = -50V$, $V_{GS} = 0V$ (2)
		—	—	−100	nA	$T_j = 25°C$ $V_{DS} = -25V$, $V_{GS} = 0V$
Gate-source leakage current	I_{GSS}	—	−1	−10	nA	$V_{GS} = \pm 20V$ $V_{DS} = 0V$
Drain-source on-state resistance (1)	$R_{DS(on)}$	—	6	10	Ω	$V_{GS} = -5V$ $I_D = -100mA$
Forward transconductance (1) (2)	g_{fs}	0.05	0.07	—	S	$V_{DS} = -25V$ $I_D = -100mA$
Input capacitance (2)	C_{iss}	—	40	—	pF	$V_{GS} = 0V$
Output capacitance (2)	C_{oss}	—	15	—		$V_{DS} = -25V$
Reverse transfer capacitance (2)	C_{rss}	—	6	—		$f = 1MHz$
Turn-on time t_{on}	$t_{d(on)}$	—	10	—	ns	$V_{DD} = -30V$
($t_{on} = t_{d(on)} + t_r$) (2)	t_r	—	10	—		$I_D = -0.27A$
Turn-off time t_{off}	$t_{d(off)}$	—	18	—		$V_{GS} = -5V$
($t_{off} = t_{d(off)} + t_f$) (2)	t_f	—	25	—		$R_{GS} = 50Ω$

Notes (1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.
(2) Sample test.

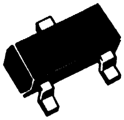
N-channel enhancement mode vertical DMOS FET

PROVISIONAL DATA

BSS123

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



SOT-23

DESCRIPTION

A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
BSS123	100V	170mA	6Ω

BSS123

ABSOLUTE MAXIMUM RATINGS

Parameters		SOT-23	Unit
V_{DS}	Drain-source voltage	100	V
I_D	Continuous drain current (@ $T_A = 25°C$)	170	mA
I_{DM}	Pulsed drain current	680	mA
V_{GS}	Gate-source voltage	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.36	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25°C$ unless otherwise stated).

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-source breakdown voltage	BV_{DSS}	100	—	—	V	$I_D = 0.25mA$, $V_{GS} = 0V$
Gate-source threshold voltage	$V_{GS(th)}$	0.8	2.2	2.8	V	$I_D = 1 mA$, $V_{DS} = V_{GS}$
Zero gate voltage drain current	I_{DSS}	— — —	1 2 —	15 60 10	μA μA nA	$V_{DS}=100V$, $V_{GS}=0V$, $T = 25°C$ $V_{DS}=100V$, $V_{GS}=0V$, $T=125°C$ (2) $V_{DS}=20V$, $V_{GS}=0V$, $T = 25°C$
Gate-body leakage	I_{GSS}	—	10	50	nA	$V_{GS} = 20V$, $V_{DS} = 0V$
Static drain-source on-state resistance (1)	$R_{DS(on)}$	—	5	6	Ω	$I_D = 100mA$, $V_{GS} = 10V$
Forward transconductance (1) and (2)	g_{fs}	80	120	—	mS	$V_{DS} = 25V$, $I_D = 100mA$
Input capacitance (2)	C_{iss}	—	20	—	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1 MHz
Common source output capacitance (2)	C_{oss}	—	9	—	pF	
Reverse transfer capacitance (2)	C_{rss}	—	4	—	pF	
Turn-on delay time (2) (3)	$t_{d(on)}$	—	10	—	ns	$V_{DD} = 30V$, $I_D = 280mA$
Rise time (2) (3)	t_r	—	10	—	ns	
Turn-off delay time (2) (3)	$t_{d(off)}$	—	15	—	ns	
Fall time (2) (3)	t_f	—	25	—	ns	

Notes (1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

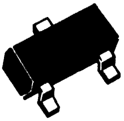
N-channel enhancement mode vertical DMOS FET

PROVISIONAL DATA

BSS138

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



SOT-23

DESCRIPTION

A compact cell geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
BSS138	50V	0.2A	3.5Ω

BSS138

ABSOLUTE MAXIMUM RATINGS

Parameters		SOT-23	Unit
V_{DS}	Drain-source voltage	50	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.2	A
I_{DM}	Pulsed drain current	0.8	A
V_{GS}	Gate-source voltage	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.36	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25°C$ unless otherwise stated).

Parameter	Symbol	Min.	Max.	Unit	Test Conditions
Drain-source breakdown voltage	BV_{DSS}	50	—	V	$I_D = 250\mu A$, $V_{GS} = 0V$
Gate-source threshold voltage	$V_{GS(th)}$	0.5	1.5	V	$I_D = 1\,mA$, $V_{DS} = V_{GS}$
Gate-body leakage	I_{GSS}	—	100	nA	$V_{GS} = 20V$, $V_{DS} = 0V$
Zero gate voltage drain current	I_{DSS}	— — —	0.5 5 100	µA µA nA	$V_{DS} = 50V$, $V_{GS} = 0V$, $T = 25°C$ $V_{DS} = 50V$, $V_{GS} = 0V$, $T = 125°C$ (2) $V_{DS} = 25V$, $V_{GS} = 0V$, $T = 25°C$
Static drain-source on-state resistance (1)	$R_{DS(on)}$	—	3.5	Ω	$I_D = 0.2A$, $V_{GS} = 5V$
Forward transconductance (1) (2)	g_{fs}	120	—	mS	$V_{DS} = 25V$, $I_D = 0.2A$
Input capacitance (2)	C_{iss}	—	50	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ $f = 1\,MHz$
Common source output capacitance (2)	C_{oss}	—	25	pF	
Reverse transfer capacitance (2)	C_{rss}	—	8	pF	
Turn-on delay time (2) (3)	$t_{d(on)}$	—	8	ns	$V_{DD} = 30V$, $I_D = 290\,mA$
Rise time (2) (3)	t_r	—	8	ns	
Turn-off delay time (2) (3)	$t_{d(off)}$	—	16	ns	
Fall time (2) (3)	t_f	—	25	ns	

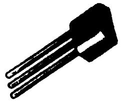
Notes (1) Measured under pulsed conditions. Width = 300µs. Duty cycle ⩽ 2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

N-channel enhancement mode vertical DMOS FET

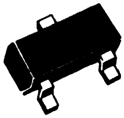
VN10L

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)
SUFFIX P



SOT-23
SUFFIX F

DESCRIPTION

A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
VN10LP	60V	0.27A	5Ω
VN10LF	60V	0.15A	5Ω

VN10L

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	SOT-23	Units
V_{DS}	Drain-source voltage	60	60	V
I_D	Continuous drain current (@ $T_A=25°C$)	0.27	0.15	A
I_{DM}	Pulsed drain current	3	3	A
V_{GS}	Gate-source voltage	±20	±20	V
P_D	Max. power dissipation (@ $T_A=25°C$)	0.625	0.25	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	60	–	V	$I_D=100\mu A$, $V_{GS}=0V$
$V_{GS(th)}$	Gate-source threshold voltage	0.8	2.5	V	$I_D=1mA$, $V_{DS}=V_{GS}$
I_{GSS}	Gate body leakage	–	100	nA	$V_{GS}=\pm 20V$, $V_{DS}=0V$
I_{DSS}	Zero gate voltage drain current	–	10	µA	V_{DS} = Max. rating, $V_{GS}=0V$
$I_{D(on)}$	On-state drain current (1)	750	–	mA	$V_{DS}=15V$, $V_{GS}=10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	5	Ω	$I_D=500mA$, $V_{GS}=10V$
		–	7.5	Ω	$I_D=200mA$, $V_{GS}=5V$
g_{fs}	Forward transconductance (1) (2)	100	–	mS	$V_{DS}=15V$, $I_D=500mA$
C_{iss}	Input capacitance (2)	–	60	pF	$V_{DS}=25V$, $V_{GS}=0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	25	pF	
C_{rss}	Reverse transfer capacitance (2)	–	5	pF	
$t_{(on)}$	Turn-on time (2) (3)	–	10	ns	$V_{DD}\approx 15V$, $I_D=0.6A$
$t_{(off)}$	Turn-off time (2) (3)	–	10	ns	

(1) Measured under pulsed conditions. Width = 300µs. Duty cycle ⩽2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

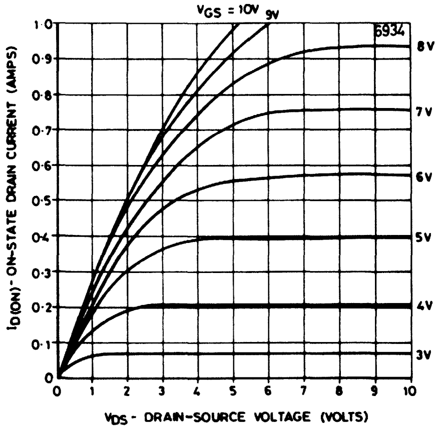


Fig. 1 Typical saturation characteristics

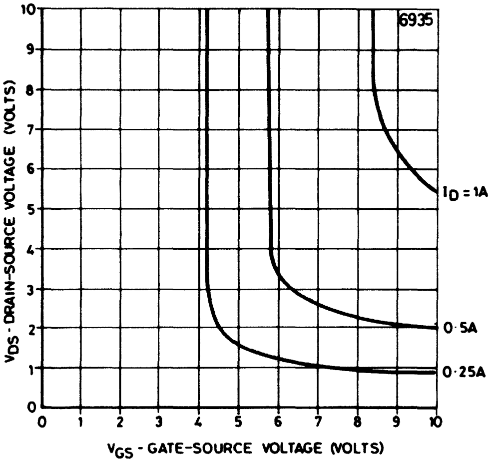


Fig. 2 Typical voltage saturation characteristics

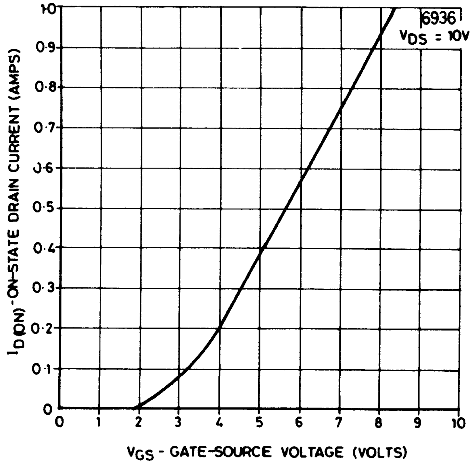


Fig. 3 Typical transfer characteristics

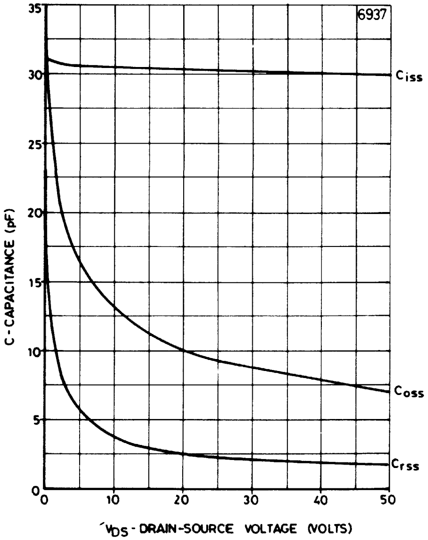


Fig. 4 Typical capacitance v drain-source voltage

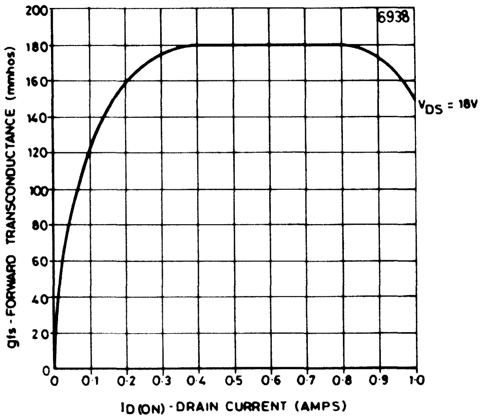


Fig. 5 Typical transconductance v drain current

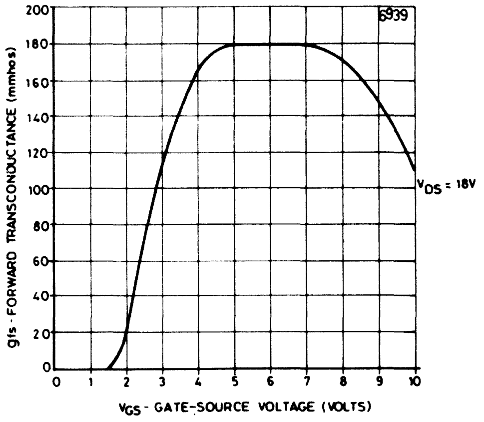


Fig. 6 Typical transconductance v gate-source voltage

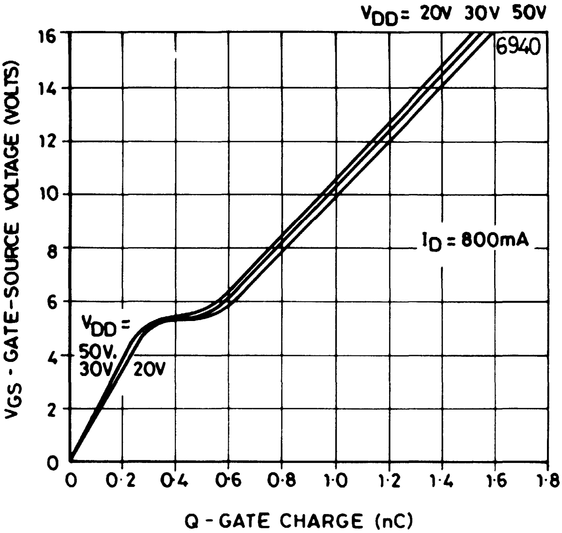


Fig. 7 Typical gate charge v gate-source voltage

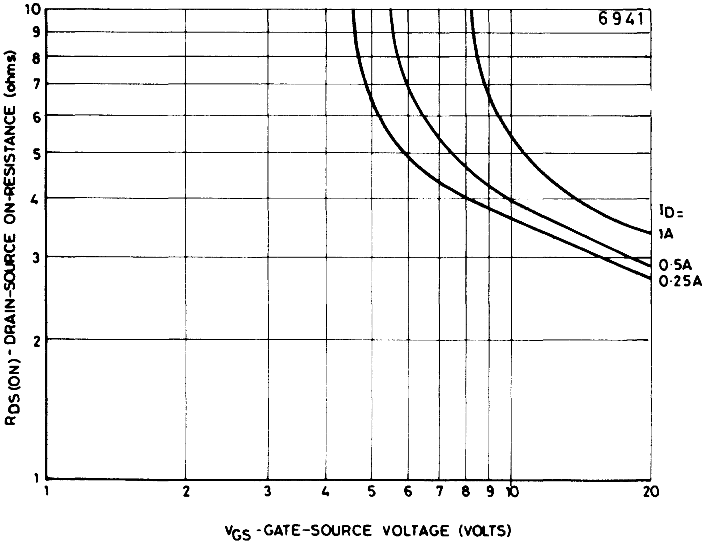


Fig. 8 Typical on-resistance v gate-source voltage

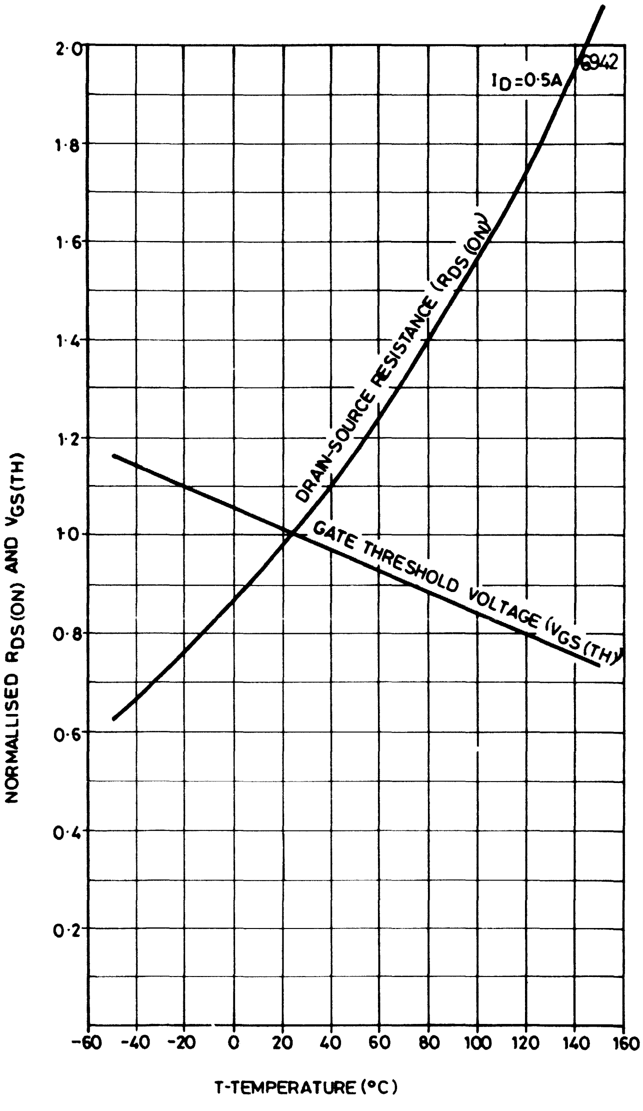


Fig. 9 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

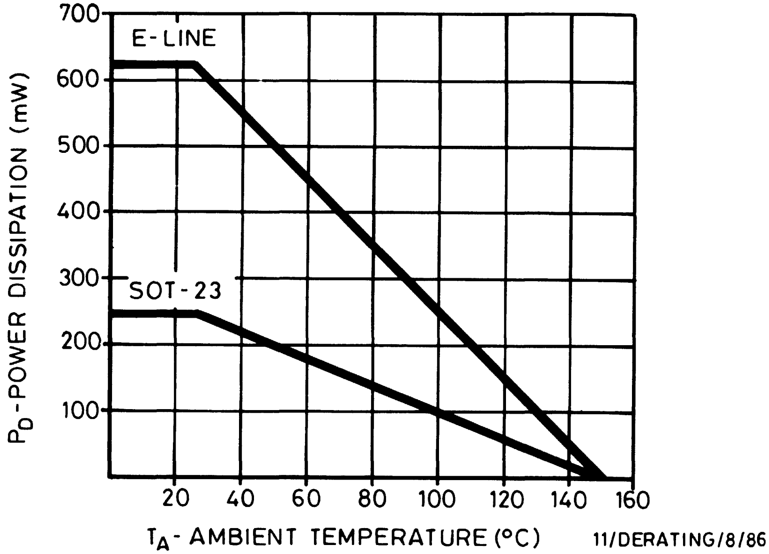


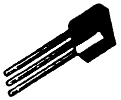
Fig. 10 Power v temperature derating curve (ambient)

N-channel enhancement mode vertical DMOS FET

ZVNL110

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)
SUFFIX A

DESCRIPTION

A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVNL110A	100V	0.32A	3Ω

ZVNL110

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	Unit
V_{DS}	Drain-source voltage	100	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.32	A
I_{DM}	Pulsed drain current	6	A
V_{GS}	Gate-source voltage	± 20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25°C$ unless otherwise stated).

Parameter	Symbol	Min.	Max.	Unit	Test Conditions
Drain-source breakdown voltage	BV_{DSS}	100	–	V	$I_D = 1\,mA$, $V_{GS} = 0V$
Gate-source threshold voltage	$V_{GS(th)}$	0.75	1.5	V	$I_D = 1\,mA$, $V_{DS} = V_{GS}$
Gate-body leakage	I_{GSS}	–	100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
Zero gate voltage drain current	I_{DSS}	– – –	10 500 –	μA μA	V_{DS} = Max. rating, $V_{GS} = 0V$ V_{DS} = 0.8xMax. rating $V_{GS} = 0V$, (T = 125°C) (2)
On-state drain current (1)	$I_{D(on)}$	750	–	mA	$V_{DS} = 25V$, $V_{GS} = 5V$
Static drain-source on-state resistance (1)	$R_{DS(on)}$	– –	4.5 3.0	Ω Ω	$I_D = 250mA$, $V_{GS} = 5V$ $I_D = 500mA$, $V_{GS} = 10V$
Forward transconductance (1)	g_{fs}	225	–	mS	$V_{DS} = 25V$, $I_D = 500mA$
Input capacitance (2)	C_{iss}	–	75	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1 MHz
Common source output capacitance (2)	C_{oss}	–	25	pF	
Reverse transfer capacitance (2)	C_{rss}	–	8	pF	
Turn-on delay time (2) (3)	$t_{d(on)}$	–	7	ns	$V_{DD} = 25V$, $I_D = 1A$, $V_{GS} = 10V$
Rise time (2) (3)	t_r	–	12	ns	
Turn-off delay time (2) (3)	$t_{d(off)}$	–	15	ns	
Fall time (2) (3)	t_f	–	13	ns	

Notes (1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.

(2) Sample test.

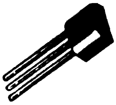
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

N-channel enhancement mode vertical DMOS FET

ZVNL120

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)
SUFFIX A or C

DESCRIPTION

A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVNL120A	200V	0.18A	10Ω
ZVNL120C	200V	0.18A	10Ω

ZVNL120

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	Unit
V_{DS}	Drain-source voltage	200	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.18	A
I_{DM}	Pulsed drain current	2	A
V_{GS}	Gate-source voltage	± 20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	W
T_j, T_{stg}	Operating/storage temperature range	-55 to $+150$	°C

ELECTRICAL CHARACTERISTICS (at $T = 25°C$ unless otherwise stated)

Parameter		Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	200	–	V	$I_D = 1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	0.5	1.5	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	10	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	100	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$, ($T = 125°C$) (2)
$I_{D(on)}$	On-state drain current (1)	500	–	mA	$V_{DS} = 25V$, $V_{GS} = 5V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	10	Ω	$I_D = 250mA$, $V_{GS} = 5V$
		–	10	Ω	$I_D = 125mA$, $V_{GS} = 3V$
g_{fs}	Forward transconductance (1) (2)	200	–	mS	$V_{DS} = 25V$, $I_D = 250mA$
C_{iss}	Input capacitance (2)	–	85	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ $f = 1MHz$
C_{oss}	Common source output capacitance (2)	–	20	pF	
C_{rss}	Reverse transfer capacitance (2)	–	7	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	8	ns	$V_{DD} \simeq 25V$, $I_D = 250mA$
t_r	Rise time (2) (3)	–	8	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	20	ns	
t_f	Fall time (2) (3)	–	12	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

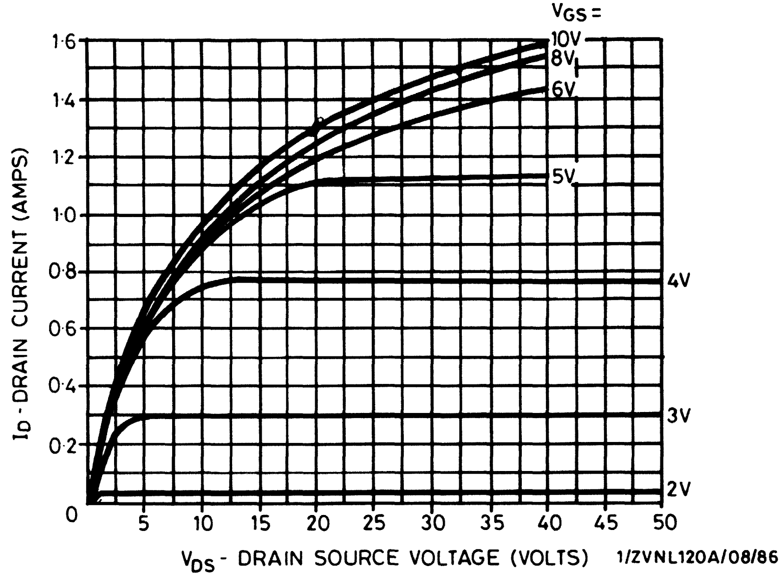


Fig. 1 Typical output characteristics

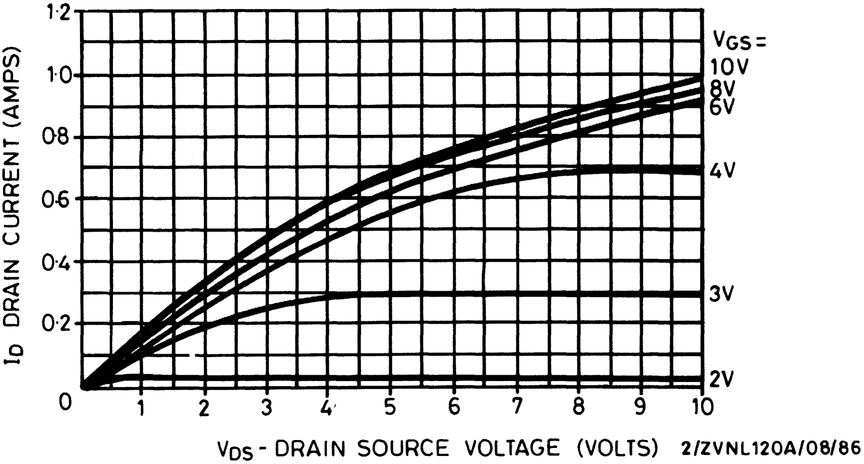


Fig. 2 Typical saturation characteristics

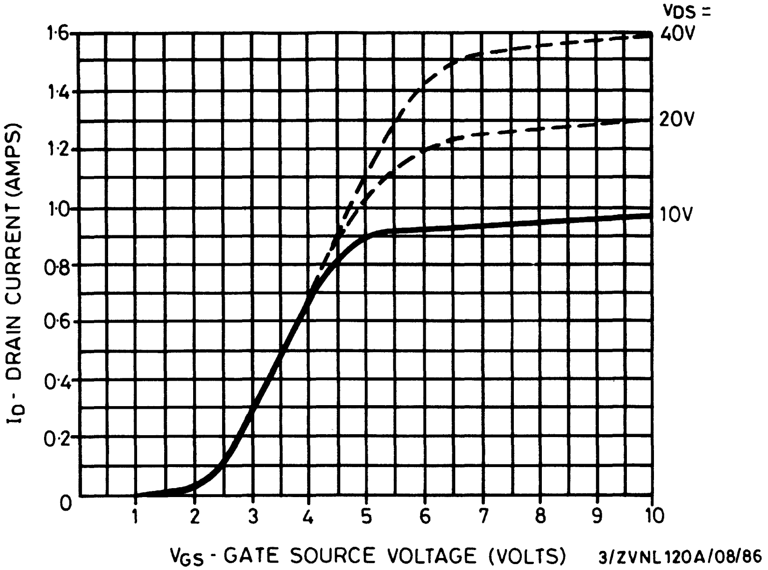


Fig. 3 Typical transfer characteristics

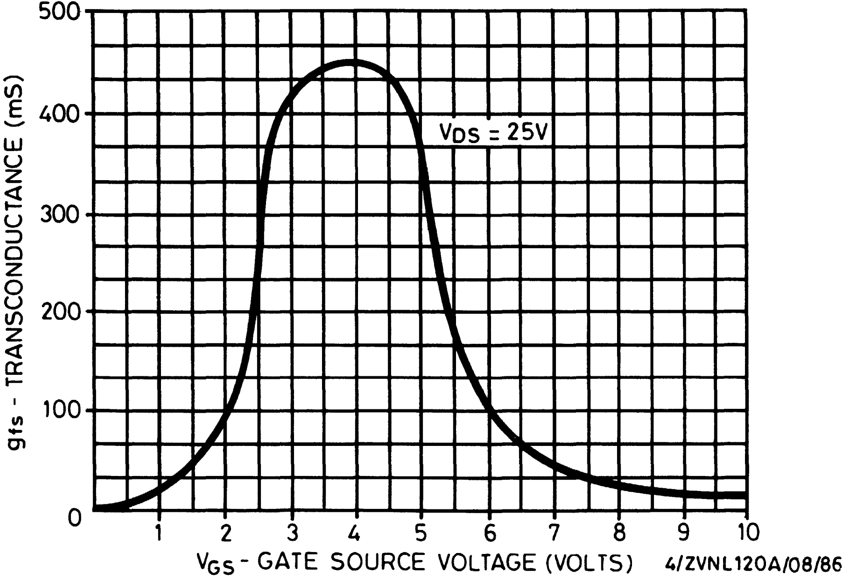


Fig. 4 Typical transconductance v gate-source voltage

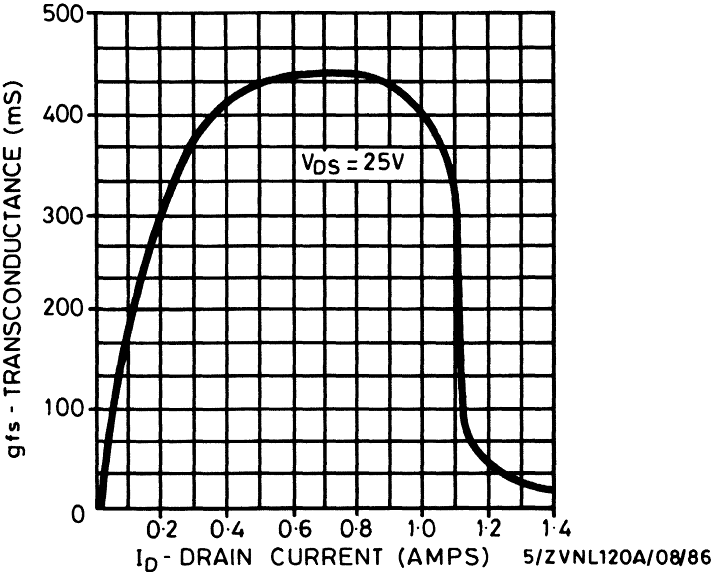


Fig. 5 Typical transconductance v drain current

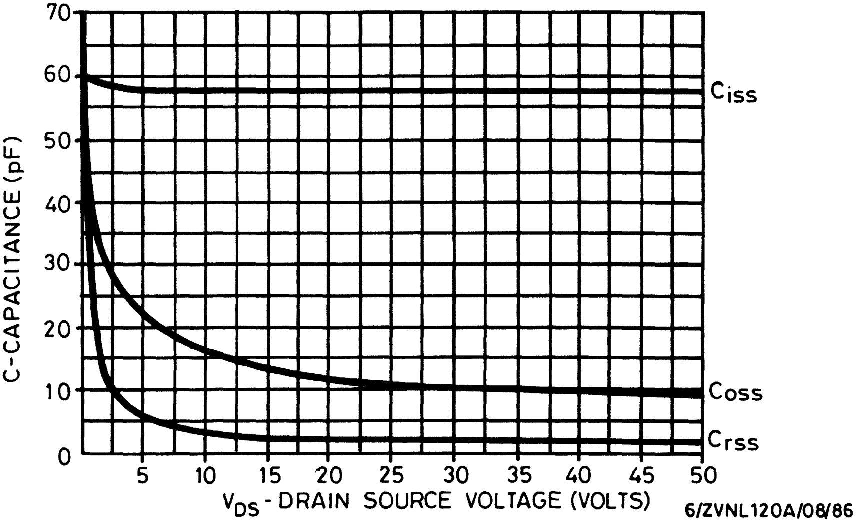


Fig. 6 Typical capacitance v drain-source voltage

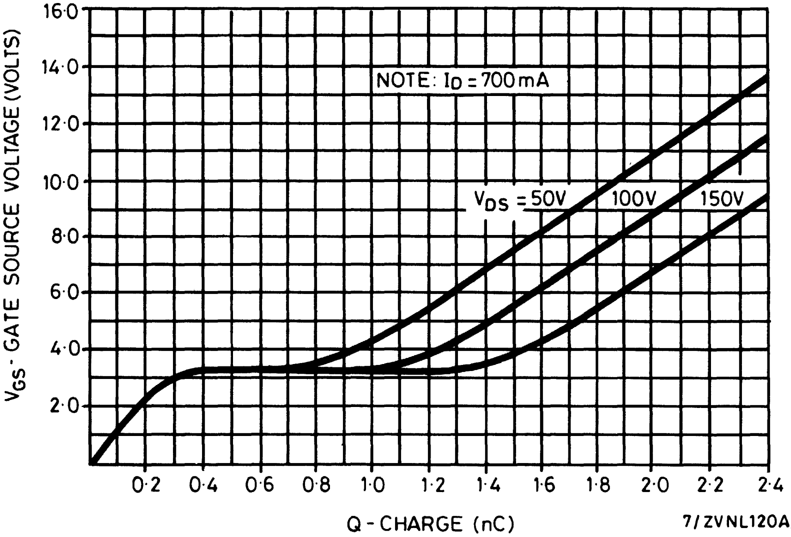


Fig. 7 Typical gate charge v gate-source voltage

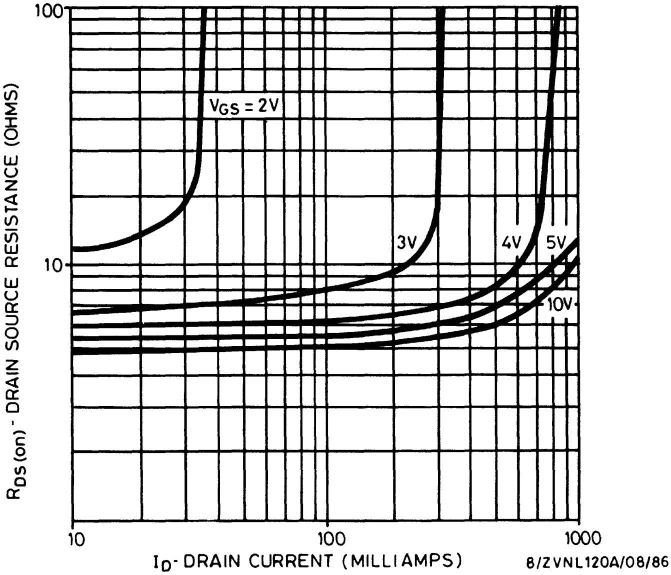
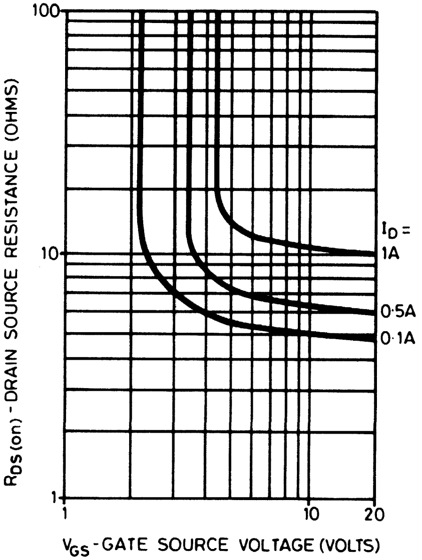
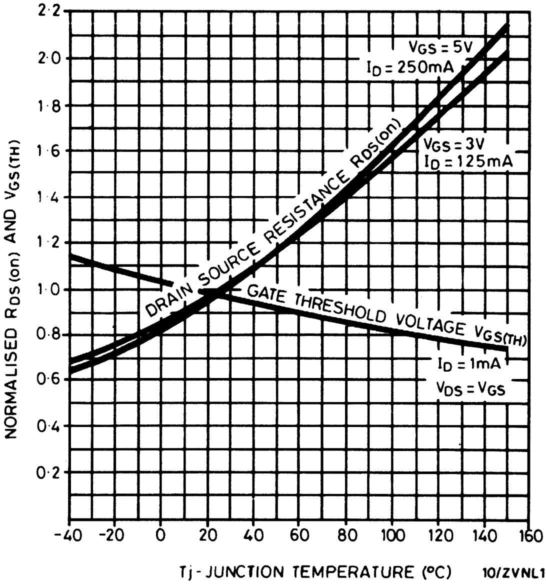


Fig. 8 Typical on-resistance v drain current



9/ZVNL120A/08/86

Fig. 9 Typical on-resistance v gate-source voltage



10/ZVNL120A/08/86

Fig. 10 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

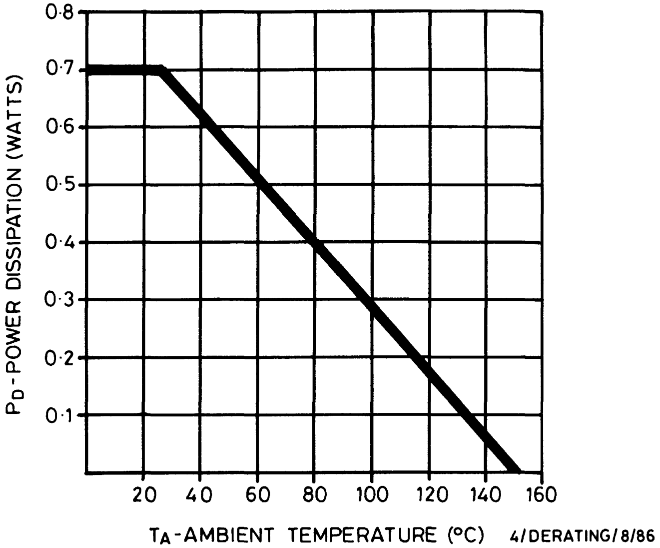


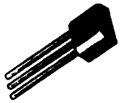
Fig. 11 Power v temperature derating curve (ambient)

N-channel enhancement mode vertical DMOS FET

ZVNL535

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)
SUFFIX A

DESCRIPTION

A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVNL535A	350V	0.09A	40Ω

ZVNL535

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	Unit
V_{DS}	Drain-source voltage	350	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.09	A
I_{DM}	Pulsed drain current	0.8	A
V_{GS}	Gate-source voltage	± 20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	W
T_j, T_{stg}	Operating/storage temperature range	-55 to $+150$	°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	350	–	V	$I_D = 1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	0.5	1.5	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	50	λA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	400	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$, $(T = 125°C)$ (2)
$I_{D(on)}$	On-state drain current (1)	200	–	mA	$V_{DS} = 25V$, $V_{GS} = 5V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	40	Ω	$I_D = 100mA$, $V_{GS} = 5V$
		–	40	Ω	$I_D = 50mA$, $V_{GS} = 3V$
g_{fs}	Forward transconductance (1) (2)	100	–	mS	$V_{DS} = 25V$, $I_D = 100mA$
C_{iss}	Input capacitance (2)	–	70	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ $f = 1MHz$
C_{oss}	Common source output capacitance (2)	–	10	pF	
C_{rss}	Reverse transfer capacitance (2)	–	4	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	7	ns	$V_{DD} \approx 25V$, $I_D = 100mA$
t_r	Rise time (2) (3)	–	7	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	16	ns	
t_f	Fall time (2) (3)	–	10	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.

(2) Sample test.

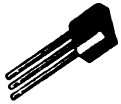
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

N-channel enhancement mode vertical DMOS FET

ZVN0117TA

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)

DESCRIPTION

A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN0117TA	170V	0.16A	23Ω

ZVN0117TA

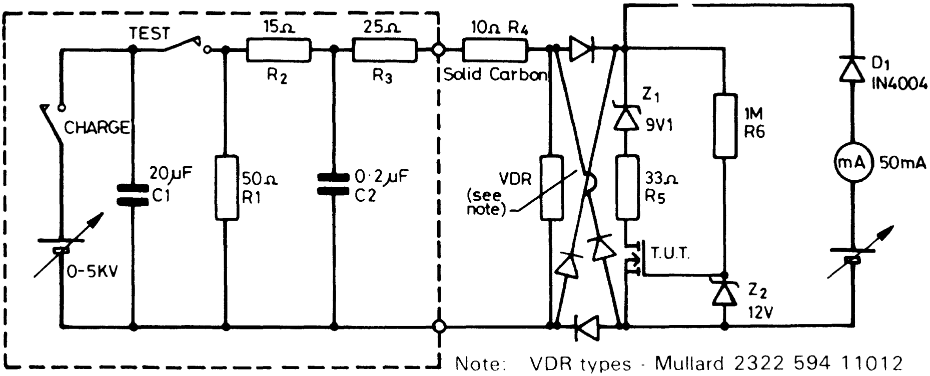
ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	Unit
V_{DS}	Drain-source voltage	170	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.16	A
I_{DM}	Pulsed drain current	2	A
V_{GS}	Gate-source voltage	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	170	–	V	$I_D = 10\mu A$, $V_{GS} = 0V$
I_{GSS}	Gate body leakage	–	100	nA	$V_{GS} = \pm 15V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	50	µA	$V_{GS} = 0V$, $V_{DS} = 140V$ $T_A = 50°C$
		(equivalent to 10µA @ 25°C)			
$I_{D(on)}$	On-state drain current (1)	100	–	mA	$V_{DS} = 3V$, $V_{GS} = 3.3V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	23	Ω	$I_D = 100mA$, $V_{GS} = 3.3V$
		–	23	Ω	$I_D = 30mA$, $V_{GS} = 3V$

(1) Measured under pulsed conditions. Width = 300µs. Duty cycle ⩽2%.



Note: VDR types - Mullard 2322 594 11012
Siemens S10V S07K 75
Matsushita ER2-C070K 10

The transistor under test should withstand a surge applied via above circuit when C1 is charged to 1.5kV.

Fig. 1 Surge test circuit

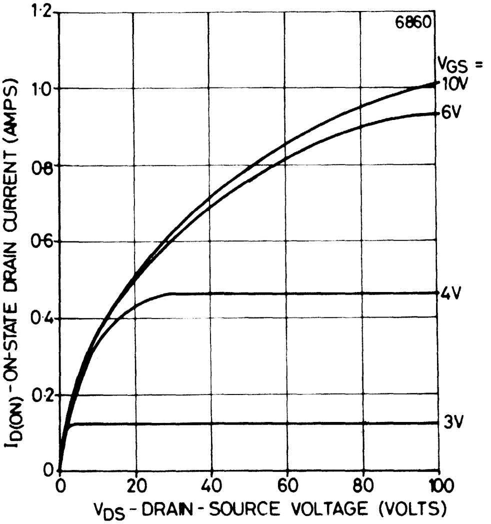


Fig. 2 Typical output characteristics

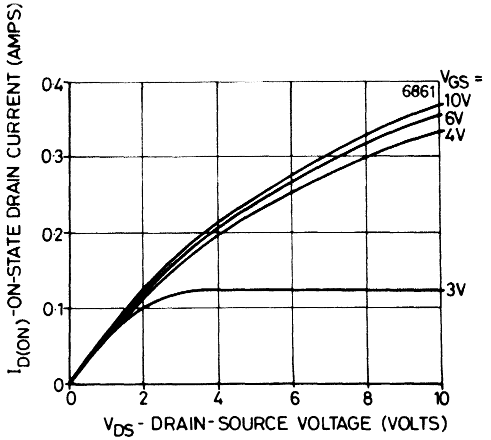


Fig. 3 Typical saturation characteristics

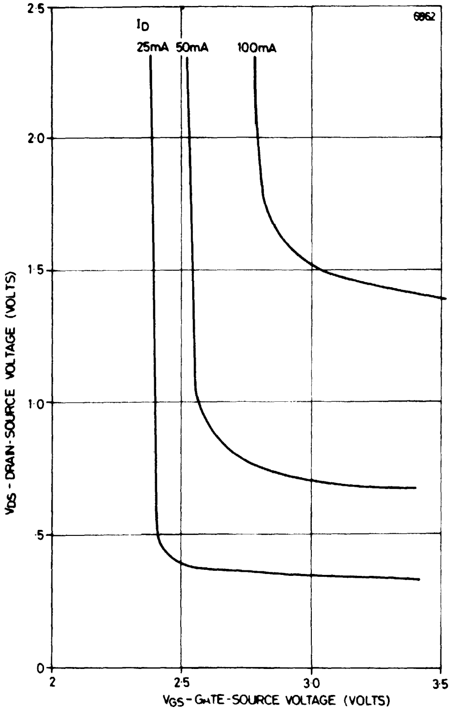


Fig. 4 Typical voltage saturation characteristics

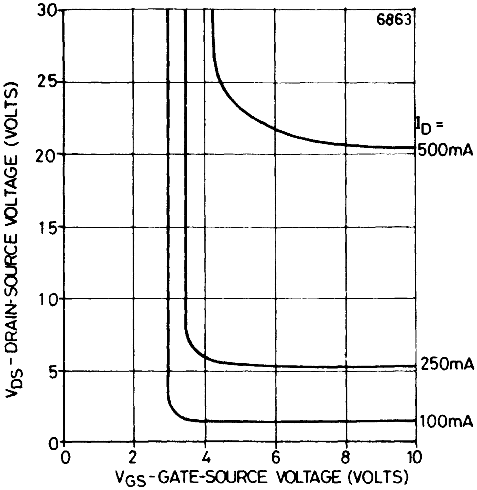


Fig. 5 Typical voltage saturation characteristics

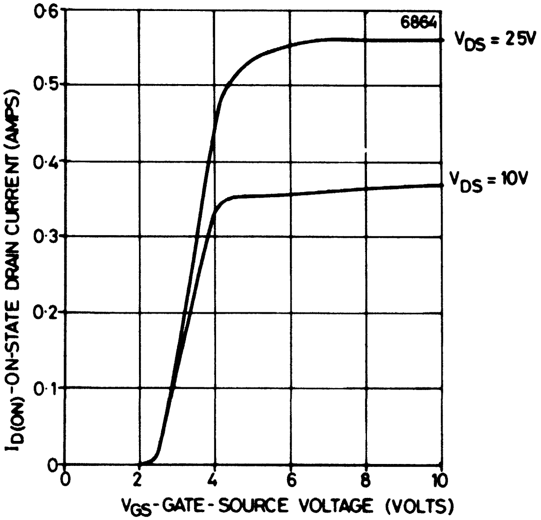


Fig. 6 Typical transfer characteristics

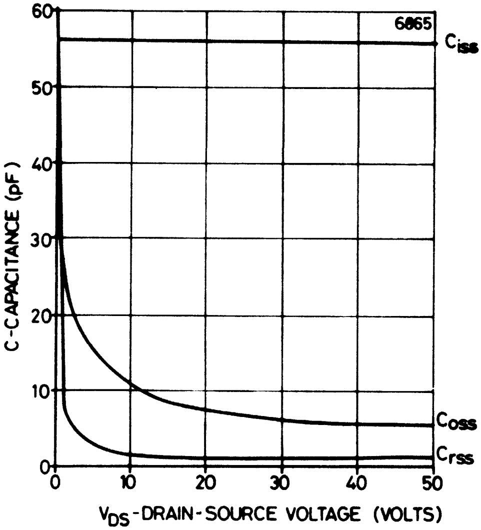


Fig. 7 Typical capacitance v drain-source voltage

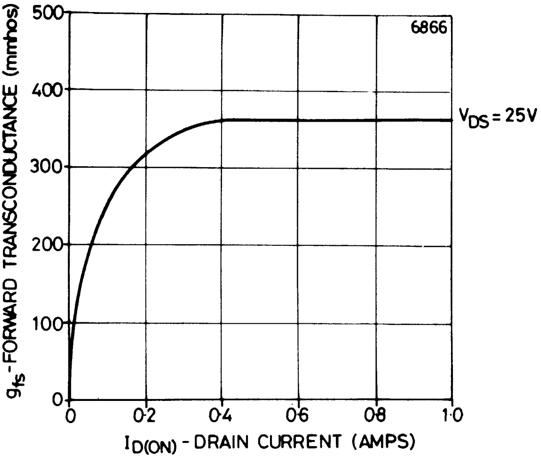


Fig. 8 Typical transconductance v drain current

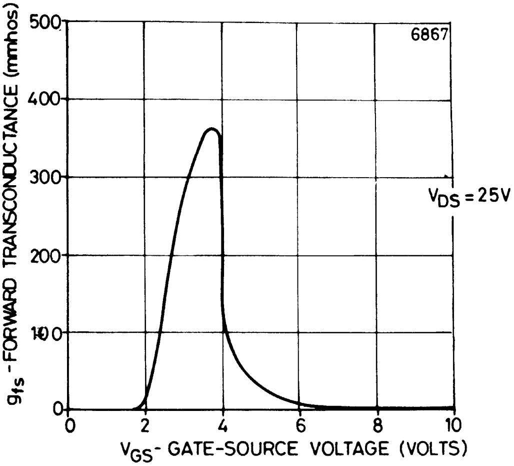


Fig. 9 Typical transconductance v gate-source voltage

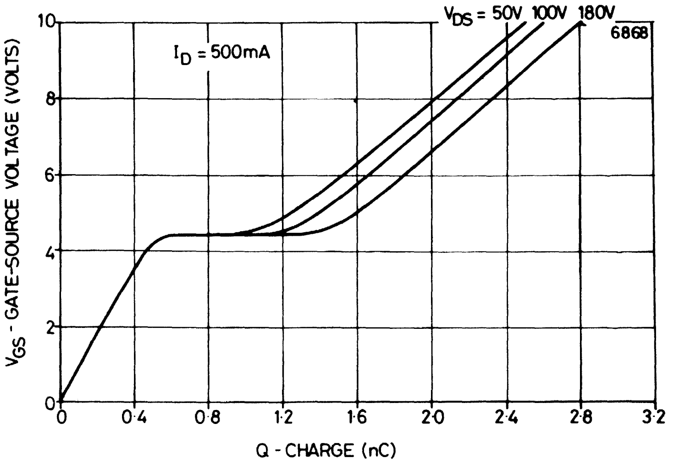


Fig. 10 Typical gate charge v gate-source voltage

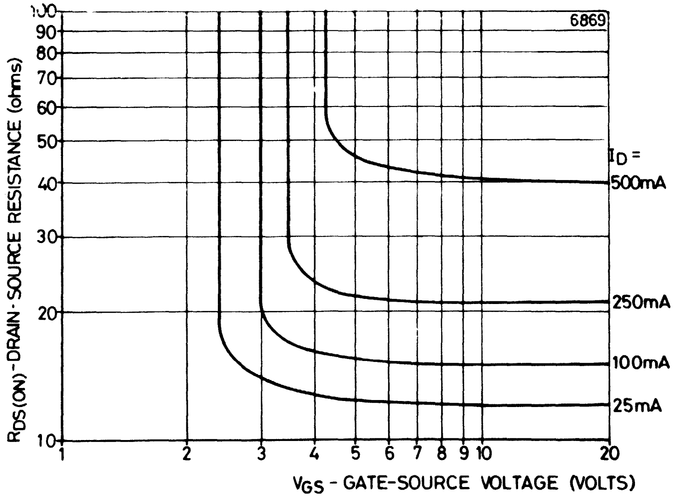


Fig. 11 Typical on-resistance v gate-source voltage

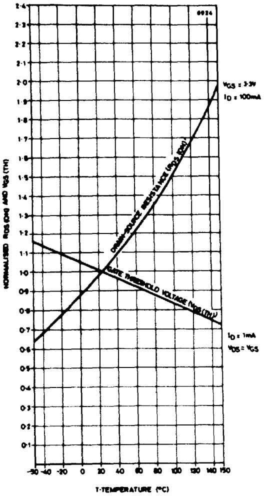


Fig. 12 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

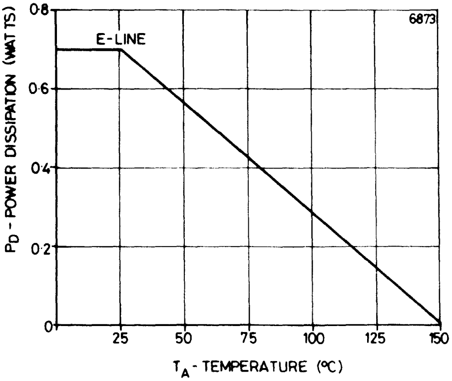


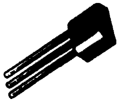
Fig. 13 Power v temperature derating curve (ambient)

N-channel enhancement-mode vertical DMOS FET

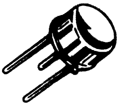
ZVN0120

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)
SUFFIX A



TO-39
SUFFIX B

DESCRIPTION

A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN0120A	200V	0.16A	16Ω
ZVN0120B	200V	0.42A	16Ω

ZVN0120

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	TO-39	Unit
V_{DS}	Drain-source voltage	200	200	V
I_D	Continuous drain current (@ $T_A=25°C$)	0.16	0.16	A
I_D	Continuous drain current (@ $T_C=25°C$)	–	0.42	A
I_{DM}	Pulsed drain current	2	2	A
V_{GS}	Gate-source voltage	±20	±20	V
P_D	Max. power dissipation (@ $T_A=25°C$)	0.7	0.7	W
P_D	Max. power dissipation (@ $T_C=25°C$)	–	5	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at $T=25°C$ unless otherwise stated)

Parameter		Min.	Typ.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	200	–	–	V	$I_D=1mA$, $V_{GS}=0V$
$V_{GS(th)}$	Gate-source threshold voltage	1	–	3	V	$I_D=1mA$, $V_{DS}=V_{GS}$
I_{GSS}	Gate body leakage	–	0.1	20	nA	$V_{GS}=\pm20V$, $V_{DS}=0V$
I_{DSS}	Zero gate voltage drain current	–	–	10	μA	V_{DS}=Max. rating, $V_{GS}=0V$
		–	–	100	μA	$V_{DS}=0.8\times$Max. rating $V_{GS}=0V$ ($T=125°C$) (2)
$I_{D(on)}$	On-state drain current (1)	0.5	1	–	A	$V_{DS}=25V$, $V_{GS}=10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	–	16	Ω	$I_D=0.25A$, $V_{GS}=10V$
g_{fs}	Forward transconductance (1) (2)	0.1	0.25	–	S	$V_{DS}=25V$, $I_D=0.25A$
C_{iss}	Input capacitance (2)	–	62	85	pF	$V_{DS}=25V$, $V_{GS}=0V$ $f=1MHz$
C_{oss}	Common source output capacitance (2)	–	9	20	pF	
C_{rss}	Reverse transfer capacitance (2)	–	2	7	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	3	7	ns	$V_{DD}\approx25V$, $I_D=0.25A$
t_r	Rise time (2) (3)	–	2	8	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	11	16	ns	
t_f	Fall time (2) (3)	–	5	8	ns	

SOURCE-DRAIN DIODE CHARACTERISTICS

	Parameter	Typ.	Unit	Conditions
V_{SD}	Forward ON voltage (1)	0.76	V	$V_{GS}=0V$, $I_S=0.16A$
t_{rr}	Reverse recovery time	105	ns	$V_{GS}=0V$, $I_F=0.16A$ $I_R=0.1A$

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽2%.

(2) Sample test.

(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

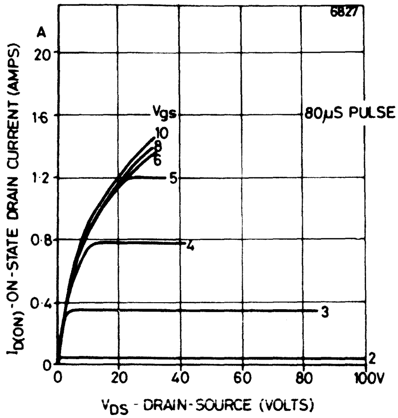


Fig. 1 Typical output characteristics

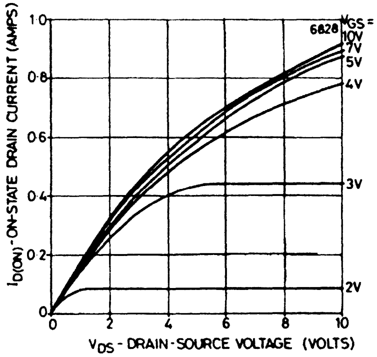


Fig. 2 Typical saturation characteristics

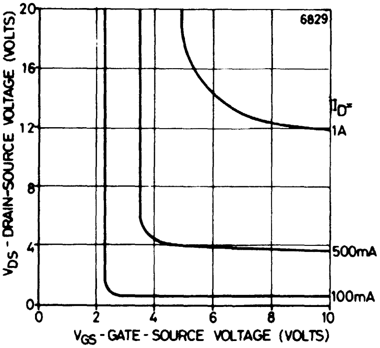


Fig. 3 Typical voltage saturation characteristics

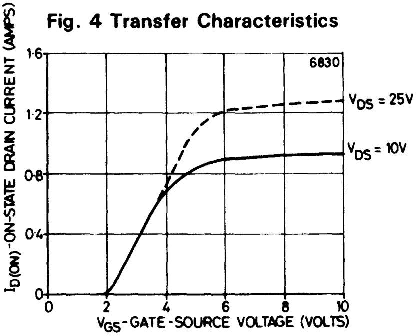


Fig. 4 Typical transfer characteristics

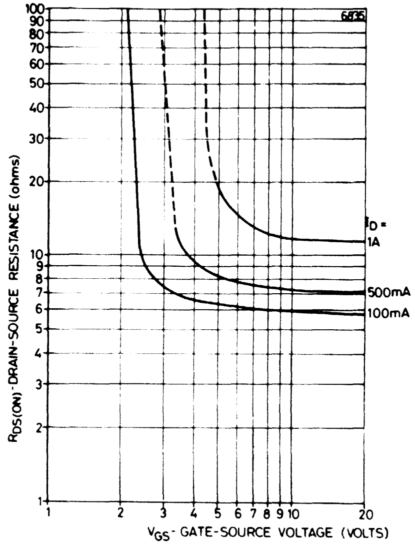


Fig. 5 Typical on-resistance v gate-source voltage

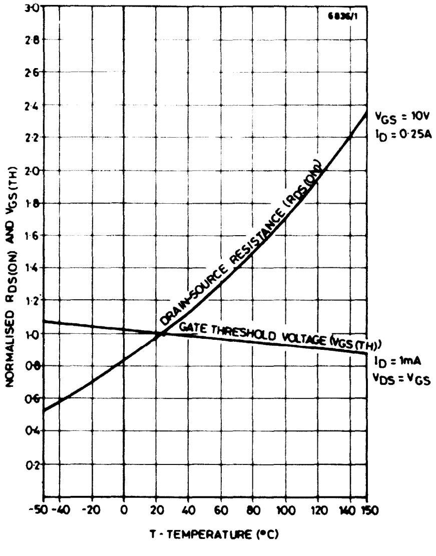


Fig. 6 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

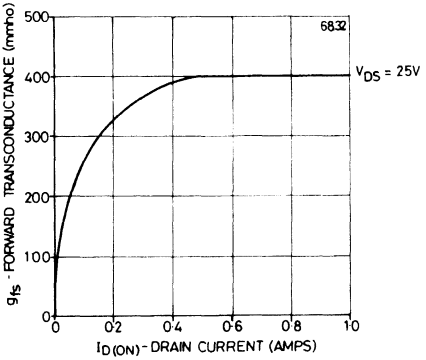


Fig. 7 Typical transconductance v drain current

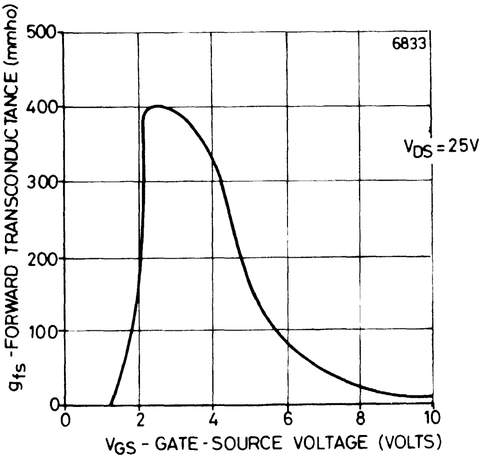


Fig. 8 Typical transconductance v gate-source voltage

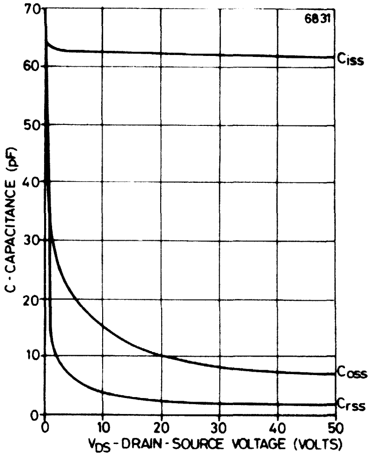


Fig. 9 Typical capacitance v drain-source voltage

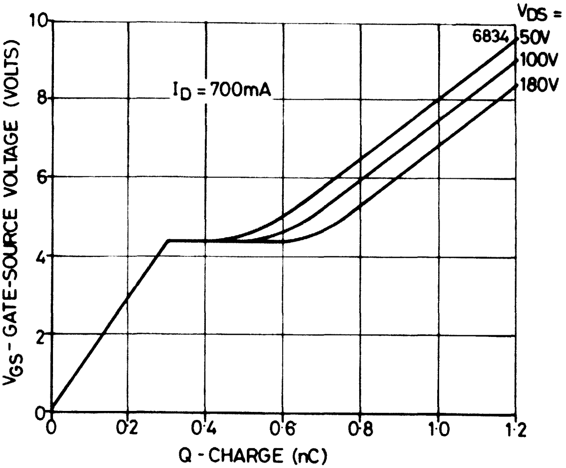


Fig. 10 Typical gate charge v gate-source voltage

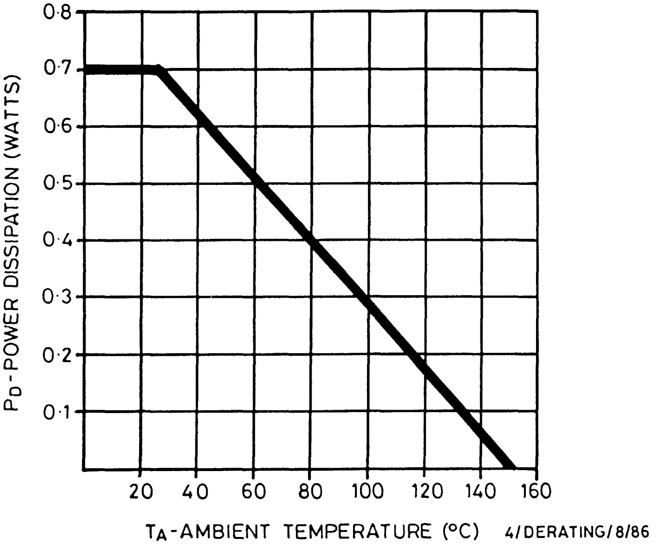


Fig. 11 Power v temperature derating curve (ambient)

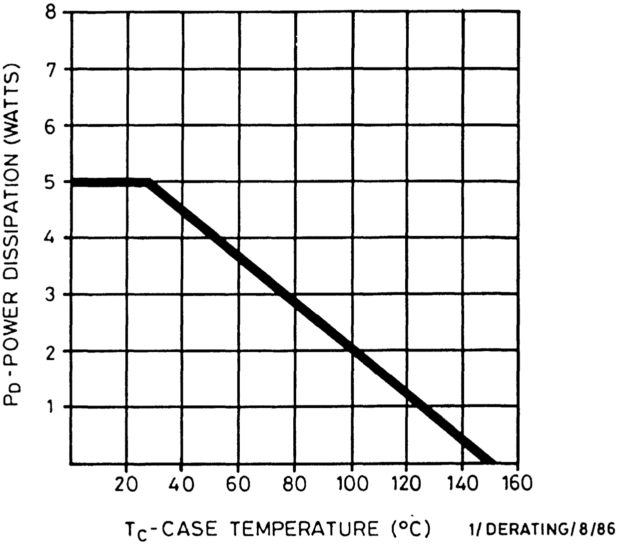


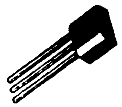
Fig. 12 Power v temperature derating curve (case)

N-channel enhancement-mode vertical DMOS FET

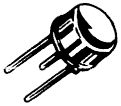
ZVN0124

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)
SUFFIX A



TO-39
SUFFIX B

DESCRIPTION

A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN0124A	240V	0.16 A	16Ω
ZVN0124B	240V	0.42 A	16Ω

ZVN0124

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	TO-39	Unit
V_{DS}	Drain-source voltage	240	240	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.16	0.16	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	0.42	A
I_{DM}	Pulsed drain current	2	2	A
V_{GS}	Gate-source voltage	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	0.7	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Typ.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	240	–	–	V	$I_D = 1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	1	–	3	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	0.1	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	–	10	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	–	100	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ ($T = 125°C$) (2)
$I_{D(on)}$	On-state drain current (1)	0.5	1	–	A	$V_{DS} = 25V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	–	16	Ω	$I_D = 0.25A$, $V_{GS} = 10V$
g_{fs}	Forward transconductance (1) (2)	0.1	0.25	–	S	$V_{DS} = 25V$, $I_D = 0.25A$
C_{iss}	Input capacitance (2)	–	62	85	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ $f = 1MHz$
C_{oss}	Common source output capacitance (2)	–	9	20	pF	
C_{rss}	Reverse transfer capacitance (2)	–	2	7	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	3	7	ns	$V_{DD} \approx 25V$, $I_D = 0.25A$
t_r	Rise time (2) (3)	–	2	8	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	11	16	ns	
t_f	Fall time (2) (3)	–	5	8	ns	

SOURCE-DRAIN DIODE CHARACTERISTICS

	Parameter	Typ.	Unit	Conditions
V_{SD}	Forward ON voltage (1)	0.76	V	$V_{GS}=0V$, $I_S=0.16A$
t_{rr}	Reverse recovery time	105	ns	$V_{GS}=0V$, $I_F=0.16A$ $I_R=0.1A$

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.

(2) Sample test.

(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

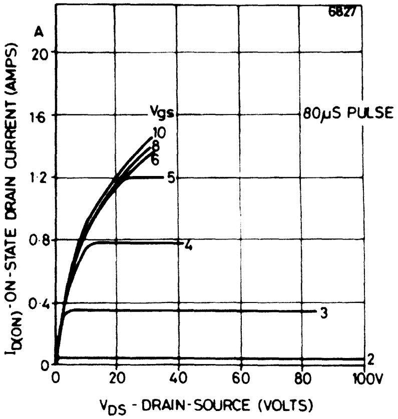


Fig. 1 Typical output characteristics

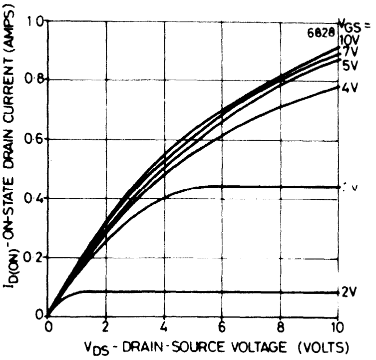


Fig. 2 Typical saturation characteristics

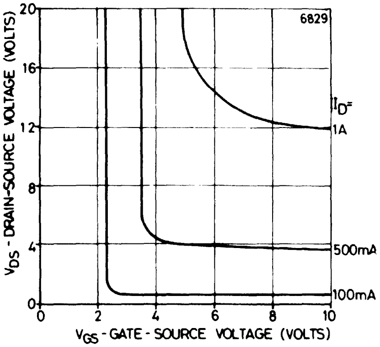


Fig. 3 Typical voltage saturation characteristics

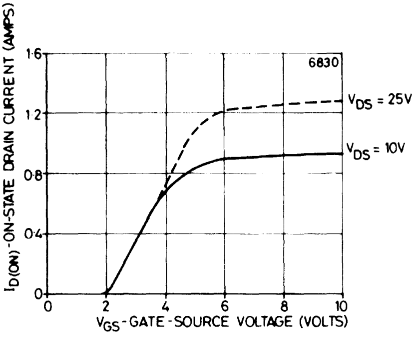


Fig. 4 Typical transfer characteristics

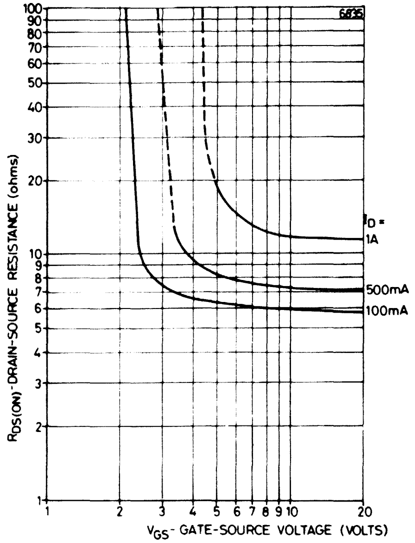


Fig. 5 Typical on-resistance v gate-source voltage

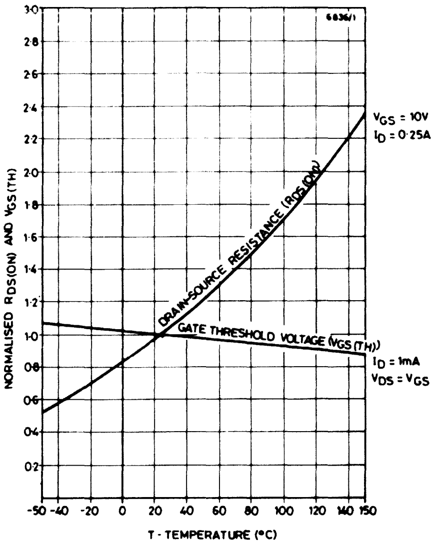


Fig. 6 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

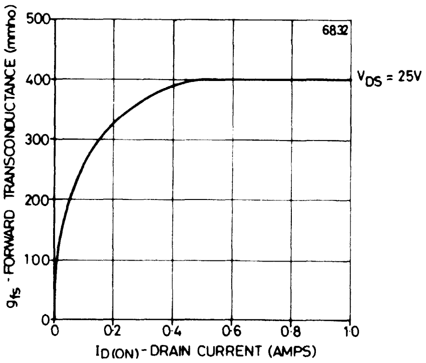


Fig. 7 Typical transconductance v drain current

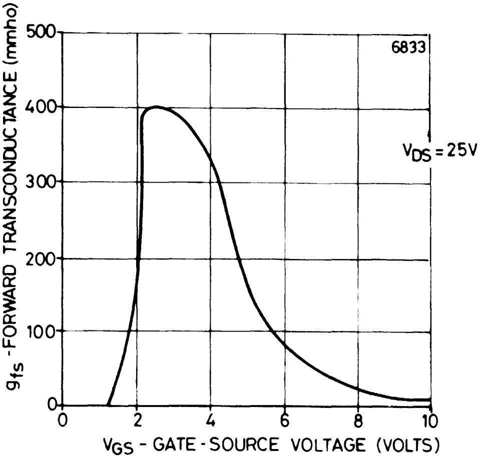


Fig. 8 Typical transconductance v gate-source voltage

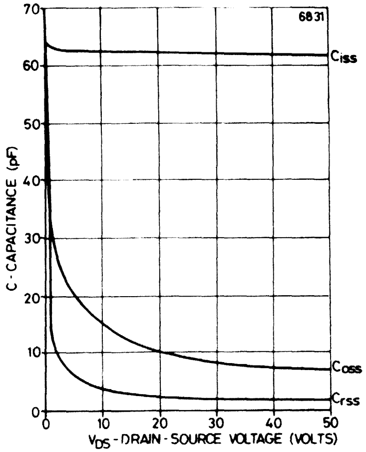


Fig. 9 Typical capacitance v drain-source voltage

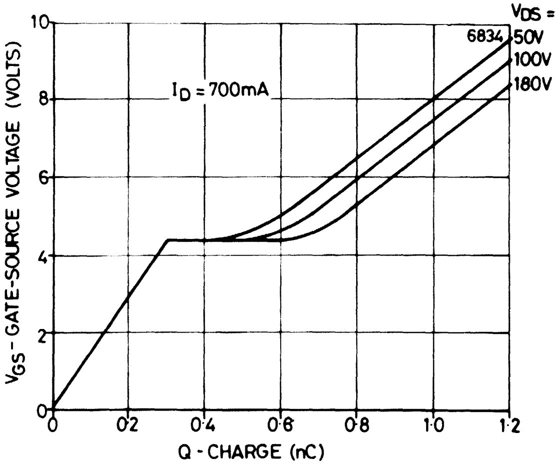


Fig. 10 Typical gate charge v gate-source voltage

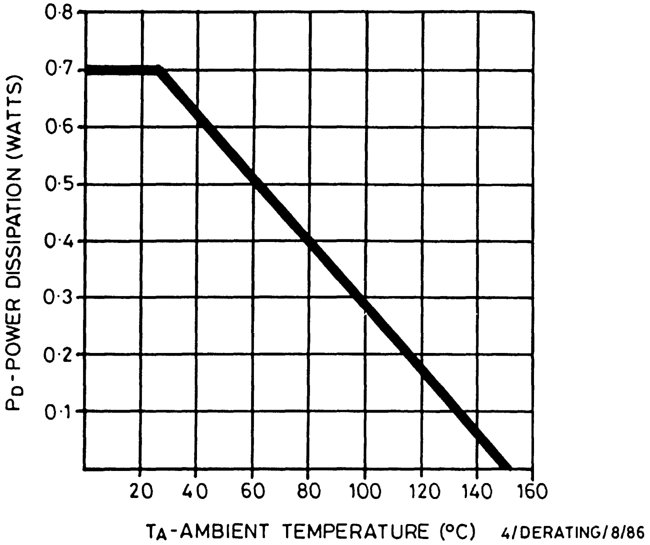


Fig. 11 Power v temperature derating curve (ambient)

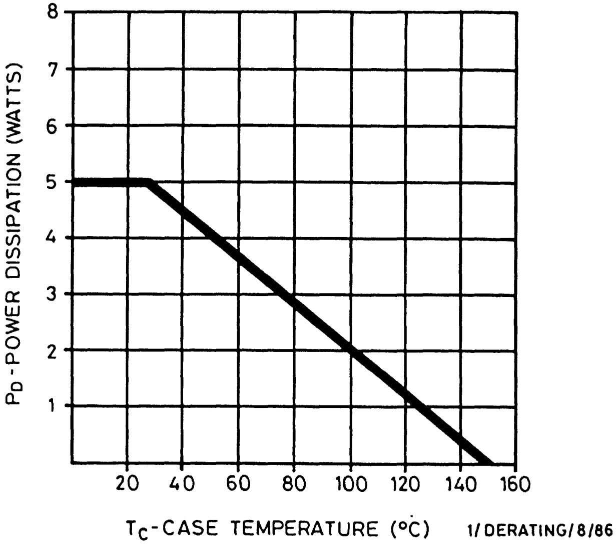


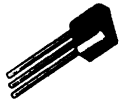
Fig. 12 Power v temperature derating curve (case)

N-channel enhancement mode vertical DMOS FET

ZVN0535

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)
SUFFIX A

DESCRIPTION

A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN0535A*	350V	90mA	50Ω

*BS-CECC approved

ZVN0535

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	Unit
V_{DS}	Drain-source voltage	350	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.09	A
I_{DM}	Pulsed drain current	0.6	A
V_{GS}	Gate-source voltage	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	350	–	V	$I_D = 1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	1	3	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	10	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	400	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ ($T = 125°C$) (2)
$I_{D(on)}$	On-state drain current (1)	150	–	mA	$V_{DS} = 25V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	50	Ω	$I_D = 100mA$, $V_{GS} = 10V$
g_{fs}	Forward transconductance (1) (2)	100	–	mS	$V_{DS} = 25V$, $I_D = 100mA$
C_{iss}	Input capacitance (2)	–	70	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	10	pF	
C_{rss}	Reverse transfer capacitance (2)	–	4	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	7	ns	$V_{DD} \approx 25V$, $I_D = 100mA$
t_r	Rise time (2) (3)	–	7	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	16	ns	
t_f	Fall time (2) (3)	–	10	ns	

SOURCE-DRAIN DIODE CHARACTERISTICS

	Parameter	Typ.	Unit	Conditions
V_{SD}	Diode forward voltage (1)	0.74	V	$V_{GS} = 0V$, $I_S = 90mA$

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽2%.

(2) Sample test.

(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

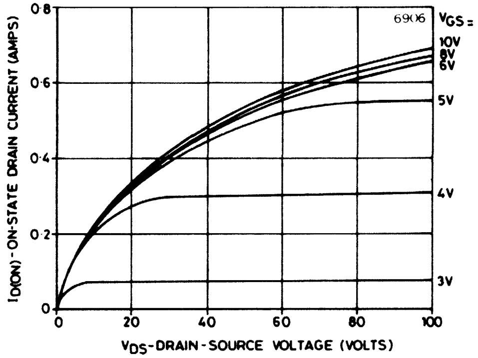


Fig. 1 Typical output characteristics

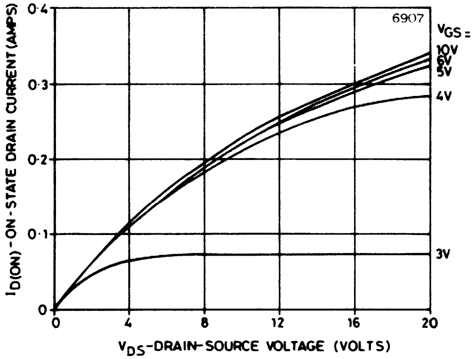


Fig. 2 Typical saturation characteristics

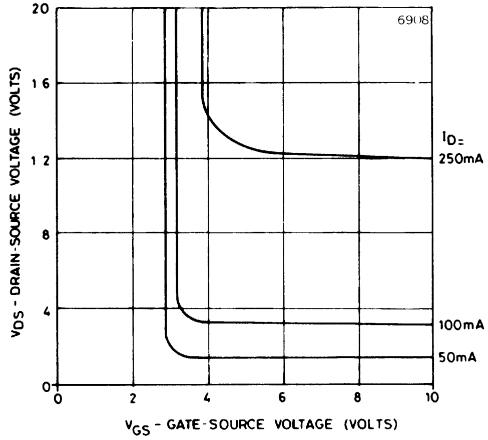


Fig. 3 Typical voltage saturation characteristics

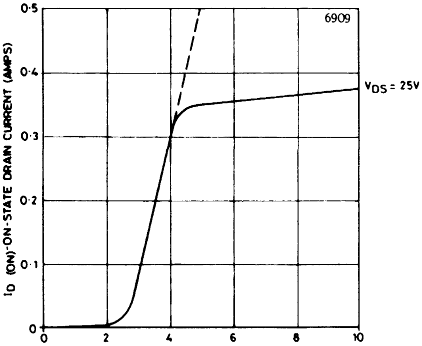


Fig. 4 Typical transfer characteristics

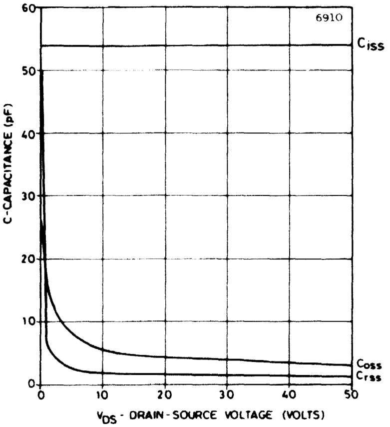


Fig. 5 Typical capacitance v drain-source voltage

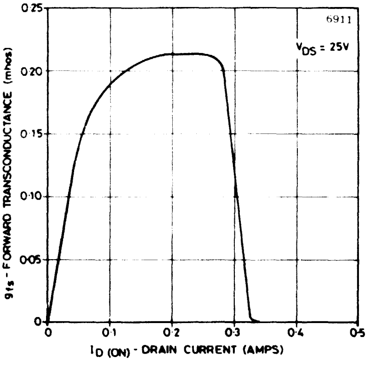


Fig. 6 Typical transconductance v drain current

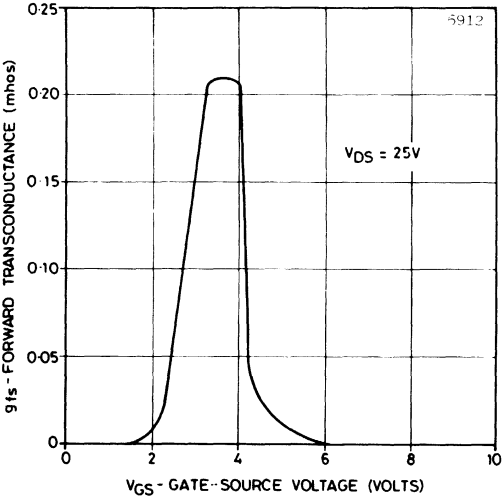


Fig. 7 Typical transconductance v gate-source voltage

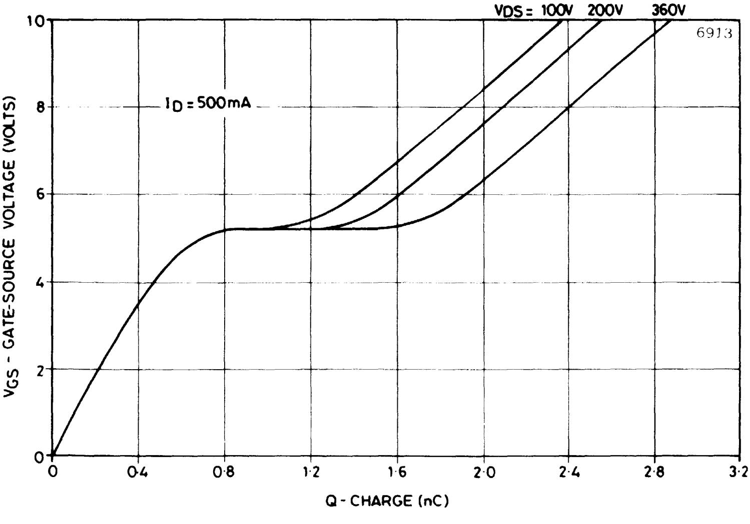


Fig. 8 Typical gate charge v gate-source voltage

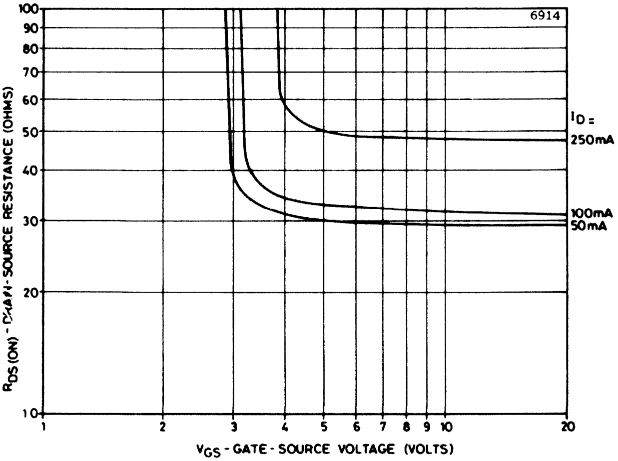


Fig. 9 Typical on-resistance v gate-source voltage

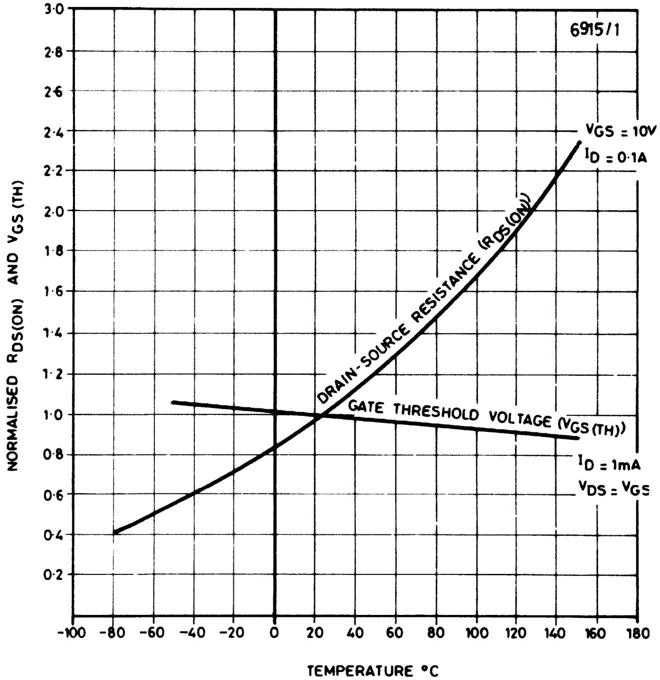


Fig. 10 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

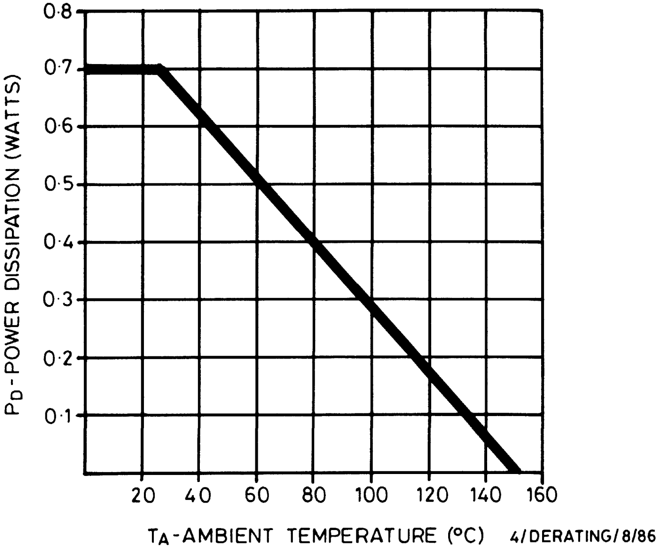


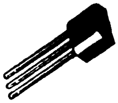
Fig. 11 Power v temperature derating curve (ambient)

N-channel enhancement-mode vertical DMOS FET

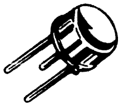
ZVN0540

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)
SUFFIX A



TO-39
SUFFIX B

DESCRIPTION

A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN0540A*	400V	0.09A	50Ω
ZVN0540B	400V	0.15A	50Ω

*BS-CECC approved

ZVN0540

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	TO-39	Unit
V_{DS}	Drain-source voltage	400	400	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.09	0.09	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	0.15	A
I_{DM}	Pulsed drain current	0.6	0.6	A
V_{GS}	Gate-source voltage	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	0.7	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	400	–	V	$I_D = 1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	1	3	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	10	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	400	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	150	–	mA	$V_{DS} = 25V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	50	Ω	$I_D = 100mA$, $V_{GS} = 10V$
g_{fs}	Forward transconductance (1) (2)	100	–	mS	$V_{DS} = 25V$, $I_D = 100mA$
C_{iss}	Input capacitance (2)	–	70	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	10	pF	
C_{rss}	Reverse transfer capacitance (2)	–	4	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	7	ns	$V_{DD} \approx 25V$, $I_D = 0.1A$
t_r	Rise time (2) (3)	–	7	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	16	ns	
t_f	Fall time (2) (3)	–	10	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.

(2) Sample test.

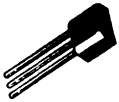
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

N-channel enhancement-mode vertical DMOS FET

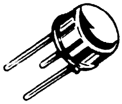
ZVN0545

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)
SUFFIX A



TO-39
SUFFIX B

DESCRIPTION

A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN0545A*	450V	0.09A	50Ω
ZVN0545B	450V	0.15A	50Ω

*BS-CECC approved

ZVN0545

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	TO-39	Unit
V_{DS}	Drain-source voltage	450	450	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.09	0.09	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	0.15	A
I_{DM}	Pulsed drain current	0.6	0.6	A
V_{GS}	Gate-source voltage	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	0.7	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	450	–	V	$I_D = 1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	1	3	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	10	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	400	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	150	–	mA	$V_{DS} = 25V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	50	Ω	$I_D = 100mA$, $V_{GS} = 10V$
g_{fs}	Forward transconductance (1) (2)	100	–	mS	$V_{DS} = 25V$, $I_D = 100mA$
C_{iss}	Input capacitance (2)	–	70	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	10	pF	
C_{rss}	Reverse transfer capacitance (2)	–	4	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	7	ns	$V_{DD} \approx 25V$, $I_D = 0.1A$
t_r	Rise time (2) (3)	–	7	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	16	ns	
t_f	Fall time (2) (3)	–	10	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.

(2) Sample test.

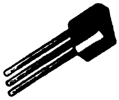
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

N-channel enhancement mode vertical DMOS FET

ZVN1409

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)
SUFFIX A

DESCRIPTION

A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN1409A	90V	10mA	250Ω

ZVN1409

ABSOLUTE MAXIMUM RATINGS

Parameter		E-line	Unit
V_{DS}	Drain-source voltage	90	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.01	A
I_{DM}	Pulsed drain current	0.04	A
V_{GS}	Gate-source voltage	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.625	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Typ.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	90	–	–	V	$I_D = 0.1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	0.8	–	2.4	V	$I_D = 0.1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate-body leakage	–	–	100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	–	1	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	–	100	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	10	–	–	mA	$V_{DS} = 25V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	–	250	Ω	$I_D = 5mA$, $V_{GS} = 10V$
g_{fs}	Forward transconductance (1) (2)	2	–	–	mS	$V_{DS} = 25V$, $I_D = 10mA$
C_{iss}	Input capacitance (2)	–	–	6.5	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	–	3	pF	
C_{rss}	Reverse transfer capacitance (2)	–	–	0.65	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	0.3	–	ns	$V_{DD} \approx 25V$, $I_D = 5mA$
t_r	Rise time (2) (3)	–	0.5	–	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	0.35	–	ns	
t_f	Fall time (2) (3)	–	0.5	–	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽2%.

(2) Sample test.

(3) Switching times measured with 50Ω source impedance on a pulse generator.

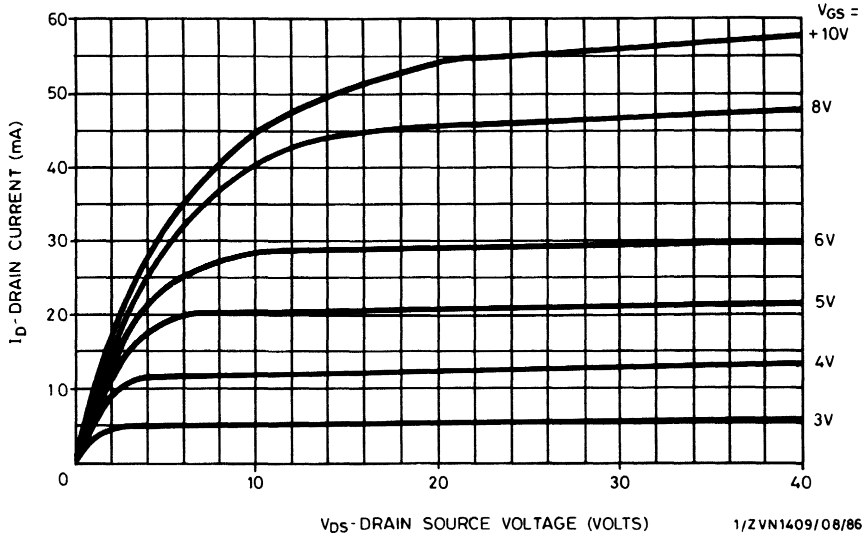


Fig. 1 Typical output characteristics

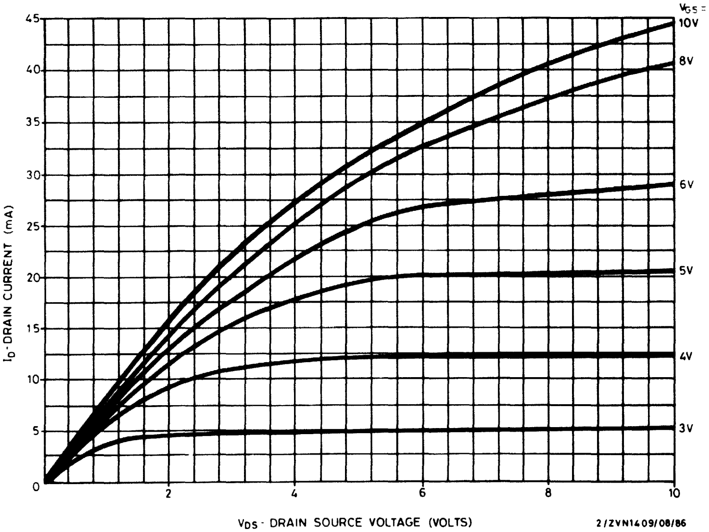


Fig. 2 Typical saturation characteristics

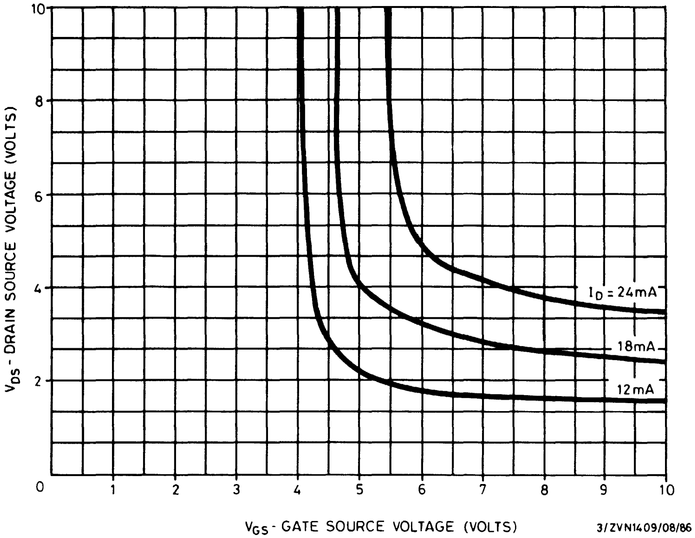


Fig. 3 Typical voltage saturation characteristics

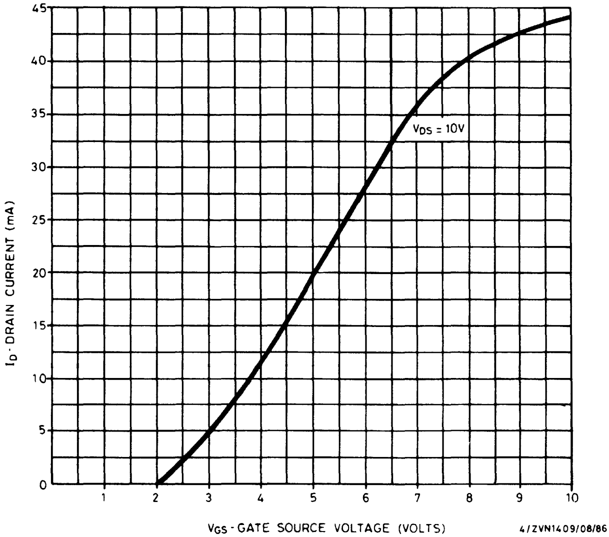


Fig. 4 Typical transfer characteristics

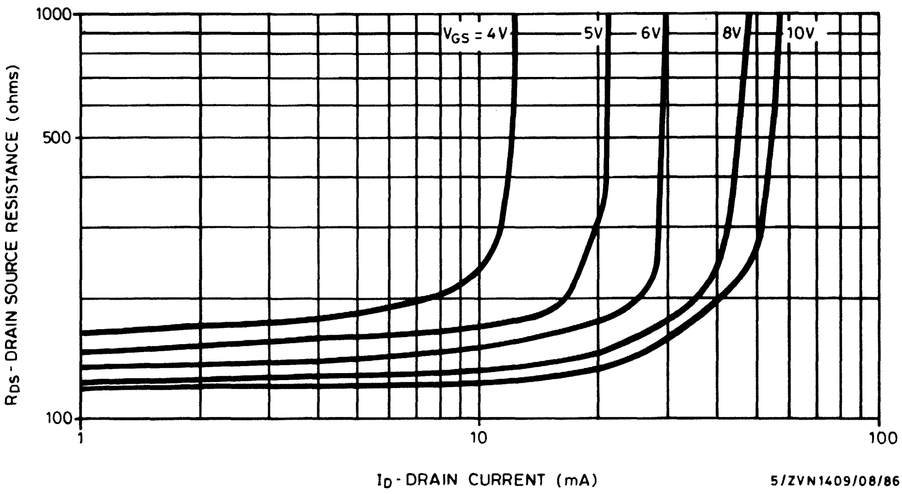


Fig. 5 Typical on-resistance v drain current

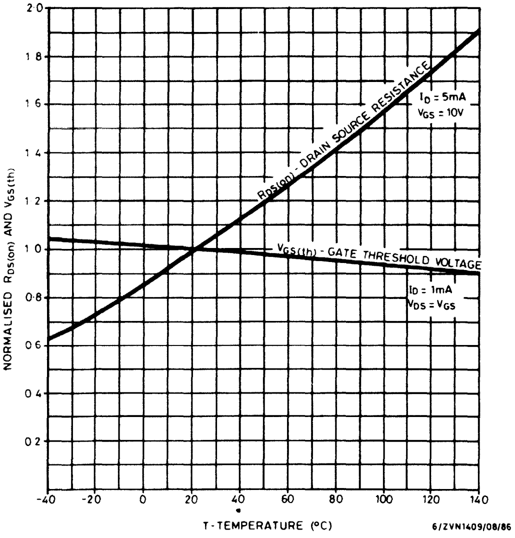


Fig. 6 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

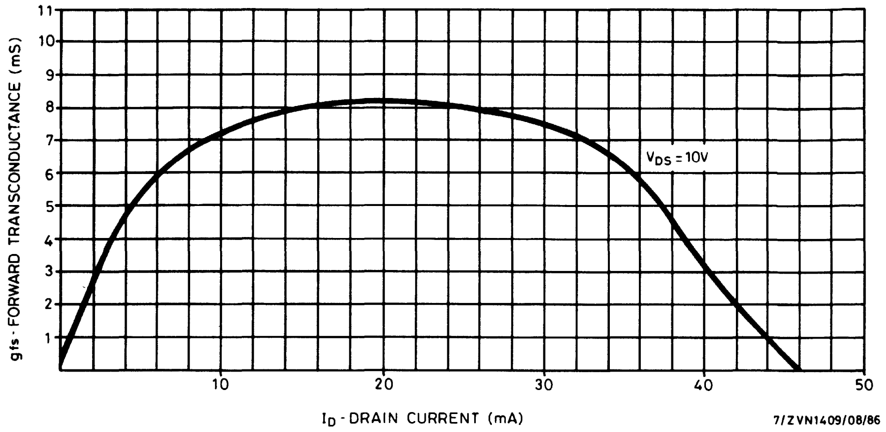


Fig. 7 Typical transconductance v drain current

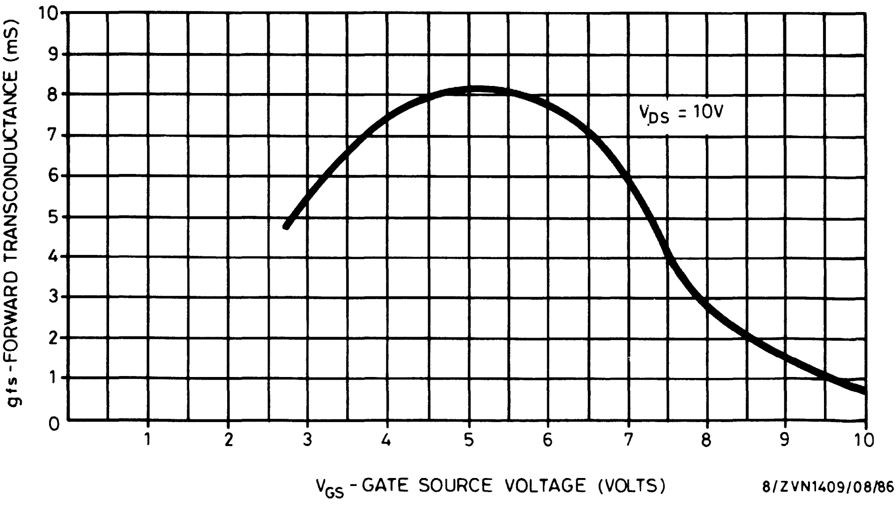


Fig. 8 Typical transconductance v gate-source voltage

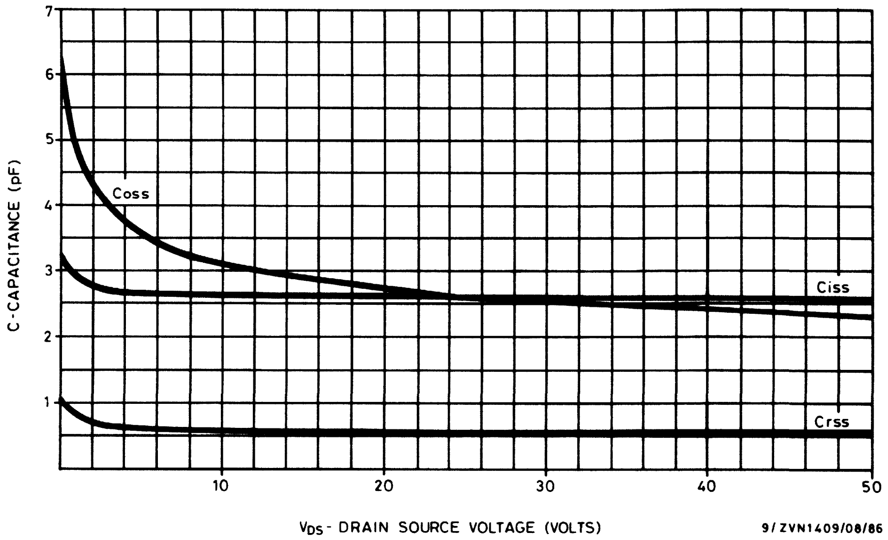


Fig. 9 Typical capacitance v drain-source voltage

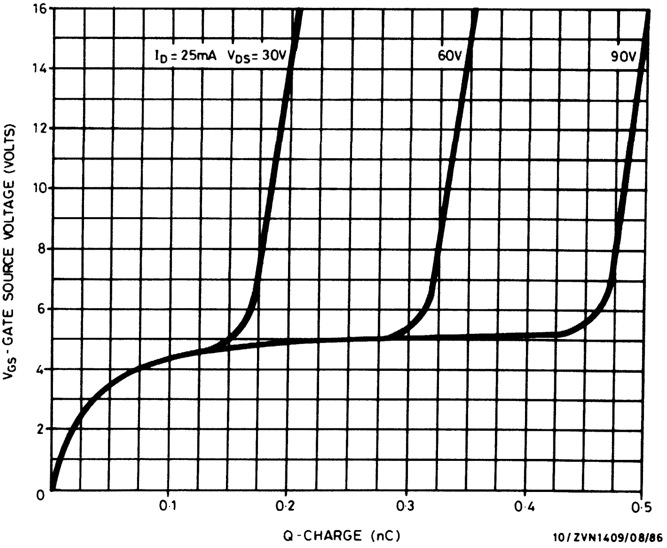


Fig. 10 Typical gate charge v gate-source voltage

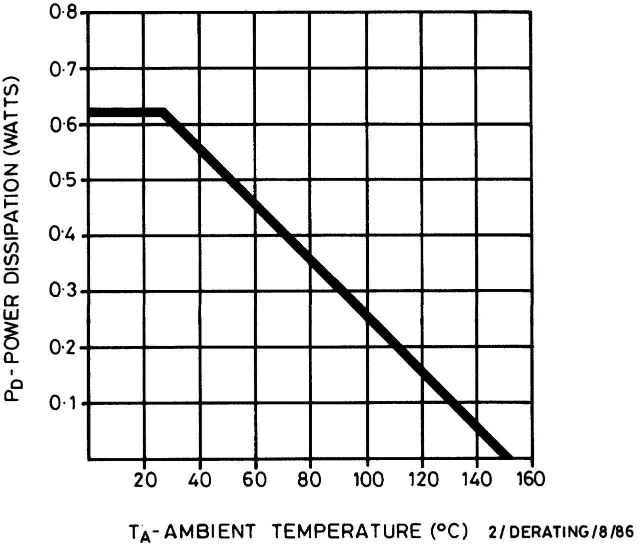


Fig. 11 Power v temperature derating curve (ambient)

N-channel enhancement mode vertical DMOS FET

ZVN2106

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling

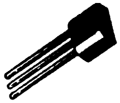
DESCRIPTION

A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

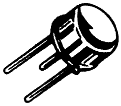
PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN2106A*	60V	0.45A	2Ω
ZVN2106B*	60V	1.2A	2Ω
ZVN2106E	60V	0.45A	2Ω
ZVN2106G	60V	0.7A	2Ω

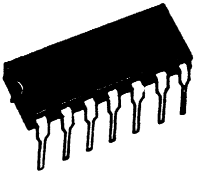
*BS-CECC approved



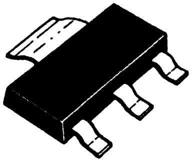
E-LINE (TO-92)
SUFFIX A



TO-39
SUFFIX B



14 LEAD MOULDED DIL
SUFFIX E



SOT-223
SUFFIX G

ZVN2106

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	TO-39	DIL	SOT-223	Units
V_{DS}	Drain-source voltage	60	60	60	60	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.45	0.45	0.45	0.7	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	1.2	–	–	A
I_{DM}	Pulsed drain current	8	8	3	8	A
V_{GS}	Gate-source voltage	±20	±20	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	0.7	0.85	2	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	–	–	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150				°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Typ.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	60	–	–	V	$I_D = 1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	0.8	–	2.4	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	0.1	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	–	0.5	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	–	0.1	mA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	2	3	–	A	$V_{DS} = 18V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	–	2	Ω	$I_D = 1A$, $V_{GS} = 10V$
g_{fs}	Forward transconductance (1) (2)	0.3	0.4	–	S	$V_{DS} = 18V$, $I_D = 1A$
C_{iss}	Input capacitance (2)	–	60	75	pF	$V_{DS} = 18V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	30	45	pF	
C_{rss}	Reverse transfer capacitance (2)	–	15	20	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	4	7	ns	$V_{DD} \approx 18V$, $I_D = 1A$
t_r	Rise time (2) (3)	–	5	8	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	8	12	ns	
t_f	Fall time (2) (3)	–	10	15	ns	

SOURCE-DRAIN DIODE CHARACTERISTICS

	Parameter	Typ.	Unit	Conditions
V_{SD}	Diode forward voltage (1)	0.82	V	$V_{GS}=0V$, $I_S=0.45A$
t_{rr}	Reverse recovery time	50	ns	$V_{GS}=0V$, $I_F=0.45A$ $I_R=0.1A$

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽2%.

(2) Sample test.

(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

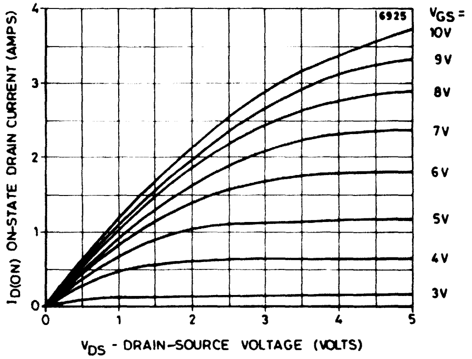


Fig. 1 Typical saturation characteristics

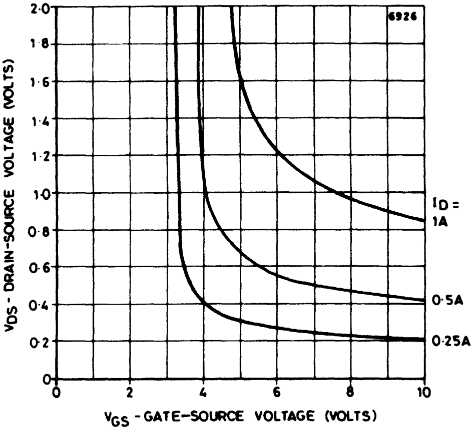


Fig. 2 Typical voltage saturation characteristics

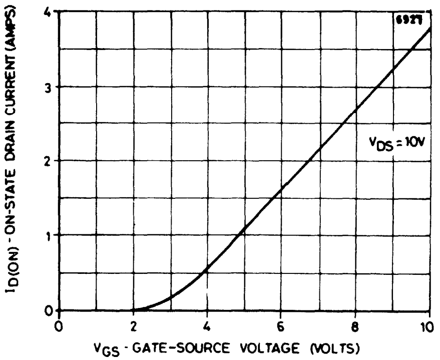


Fig. 3 Typical transfer characteristics

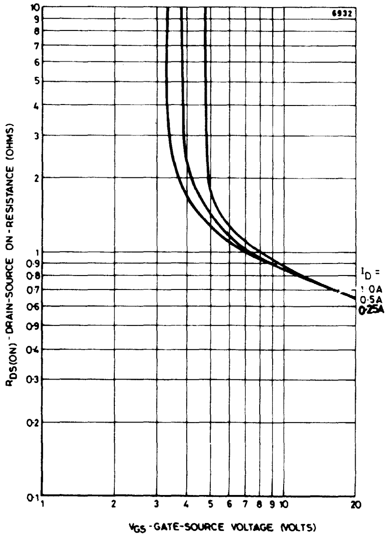


Fig. 4 Typical on-resistance v gate-source voltage

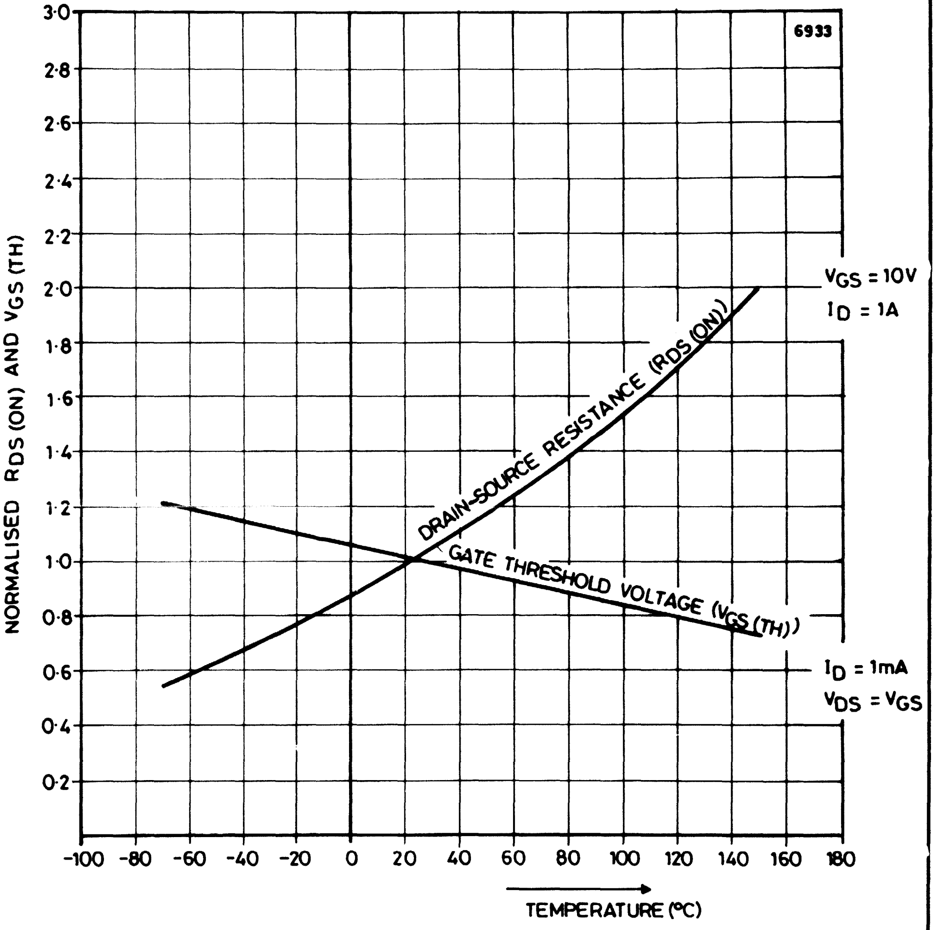


Fig. 5 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

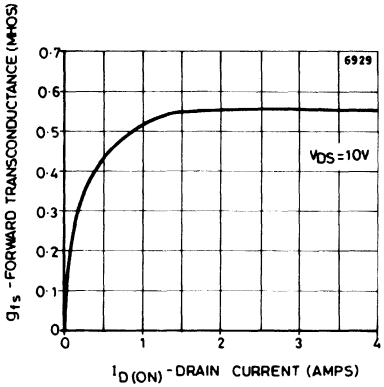


Fig. 6 Typical transconductance v drain current

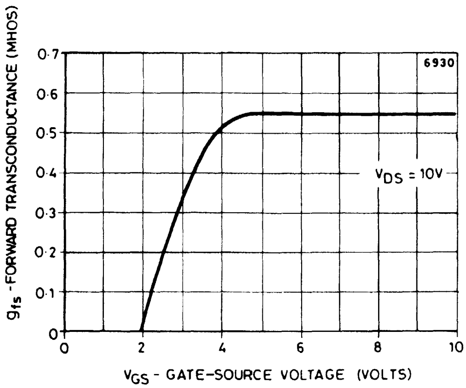


Fig. 7 Typical transconductance v gate-source voltage

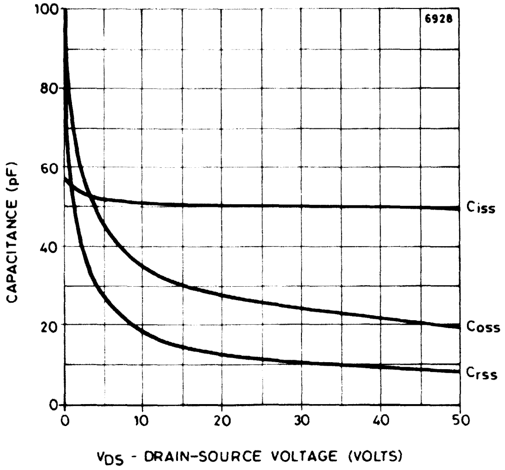


Fig. 8 Typical capacitance v drain-source voltage

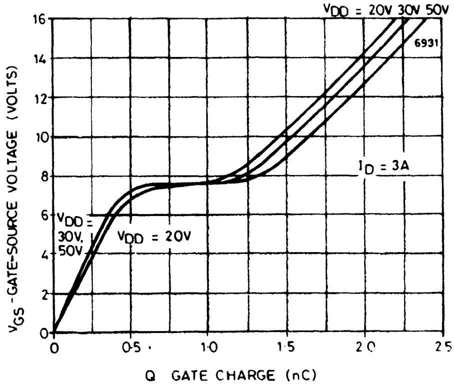


Fig. 9 Typical gate charge v gate-source voltage

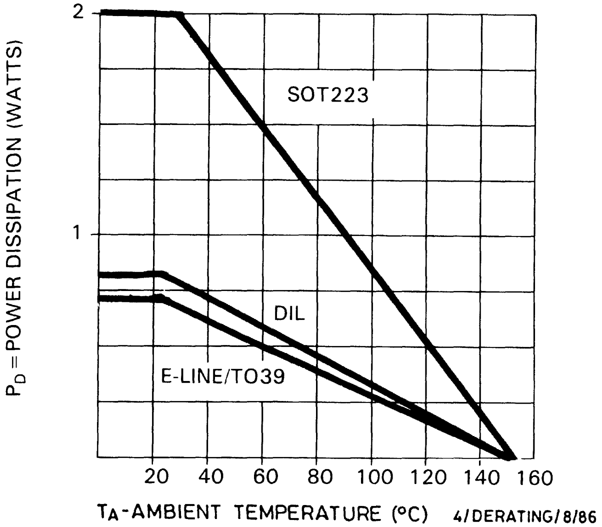


Fig. 10 Power v temperature derating curve (ambient)

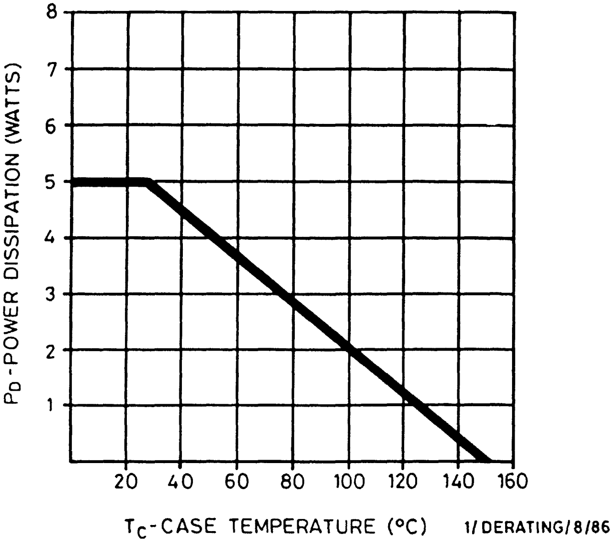


Fig. 11 Power v temperature derating curve (case)

N-channel enhancement mode vertical DMOS FET

ZVN2110

FEATURES

- **Compact geometry**
- **Fast switching speeds**
- **No secondary breakdown**
- **Excellent temperature stability**
- **High input impedance**
- **Low current drive**
- **Ease of paralleling**

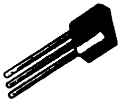
DESCRIPTION

A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

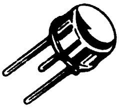
PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN2110A*	100V	0.32A	4Ω
ZVN2110B*	100V	0.85A	4Ω
ZVN2110C	100V	0.32A	4Ω
ZVN2110E	100V	0.32A	4Ω

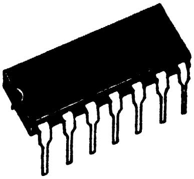
*BS-CECC approved



E-LINE (TO-92)
SUFFIX A or C



TO-39
SUFFIX B



14 LEAD MOULDED DIL
SUFFIX E

ZVN2110

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	TO-39	DIL	Units
V_{DS}	Drain-source voltage	100	100	100	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.32	0.32	0.32	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	0.85	–	A
I_{DM}	Pulsed drain current	6	6	3	A
V_{GS}	Gate-source voltage	±20	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	0.7	0.85	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	–	W
T_j, T_{stg}	Operating/storage temperature range	–55 to +150			°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Typ.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	100	–	–	V	$I_D = 1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	0.8	–	2.4	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	0.1	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	–	1	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	–	100	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ ($T = 125°C$) (2)
$I_{D(on)}$	On-state drain current (1)	1.5	2	–	A	$V_{DS} = 25V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	–	4	Ω	$I_D = 1A$, $V_{GS} = 10V$
g_{fs}	Forward transconductance (1) (2)	250	350	–	mS	$V_{DS} = 25V$, $I_D = 1A$
C_{iss}	Input capacitance (2)	–	59	75	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	16	25	pF	
C_{rss}	Reverse transfer capacitance (2)	–	4	8	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	4	7	ns	$V_{DD} \approx 25V$, $I_D = 1A$
t_r	Rise time (2) (3)	–	4	8	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	8	13	ns	
t_f	Fall time (2) (3)	–	8	13	ns	

SOURCE-DRAIN DIODE CHARACTERISTICS

	Parameter	Typ.	Unit	Conditions
V_{SD}	Diode forward voltage (1)	0.82	V	$V_{GS}=0V$, $I_S=0.32A$
t_{rr}	Reverse recovery time	112	ns	$V_{GS}=0V$, $I_F=0.32A$ $I_R=0.1A$

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

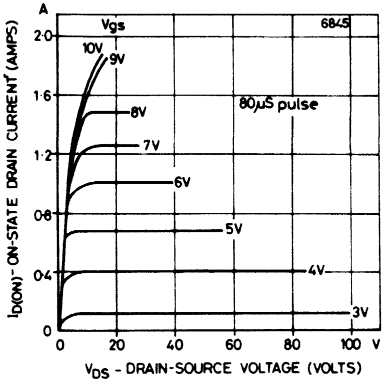


Fig. 1 Typical output characteristics

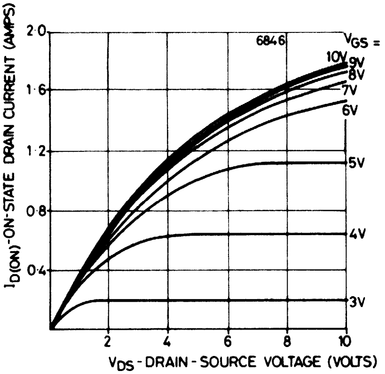


Fig. 2 Typical saturation characteristics

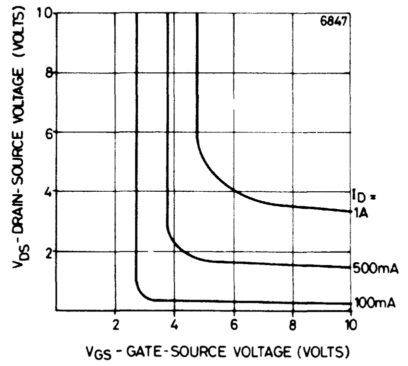


Fig. 3 Typical voltage saturation characteristics

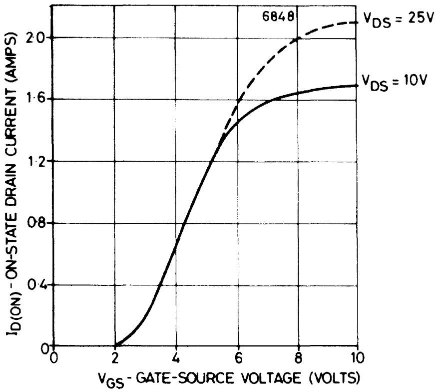


Fig. 4 Typical transfer characteristics

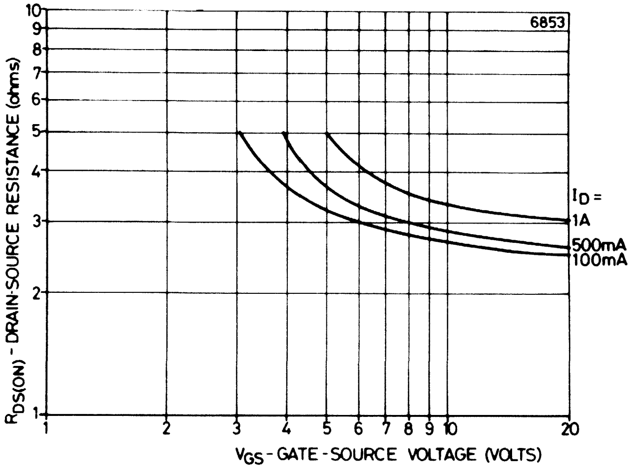


Fig. 5 Typical on-resistance v gate-source voltage

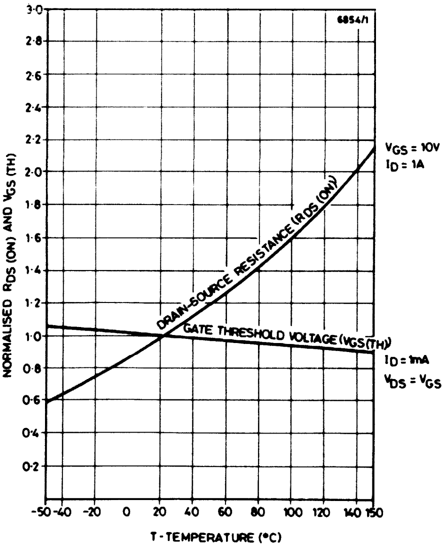


Fig. 6 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

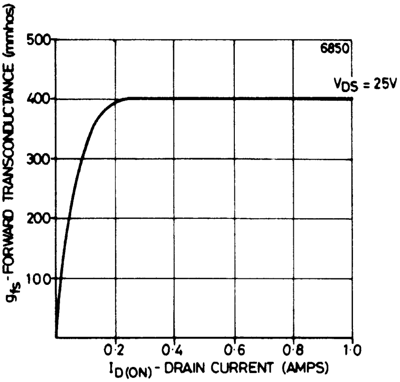


Fig. 7 Typical transconductance v drain current

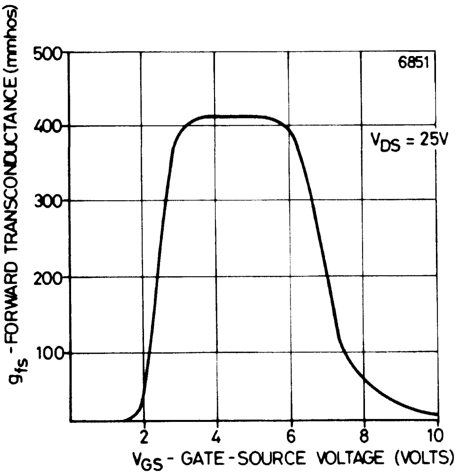


Fig. 8 Typical transconductance v gate-source voltage

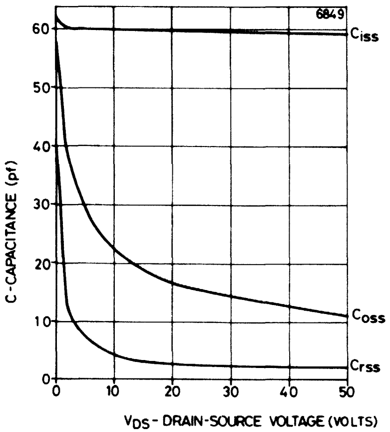


Fig. 9 Typical capacitance v drain-source voltage

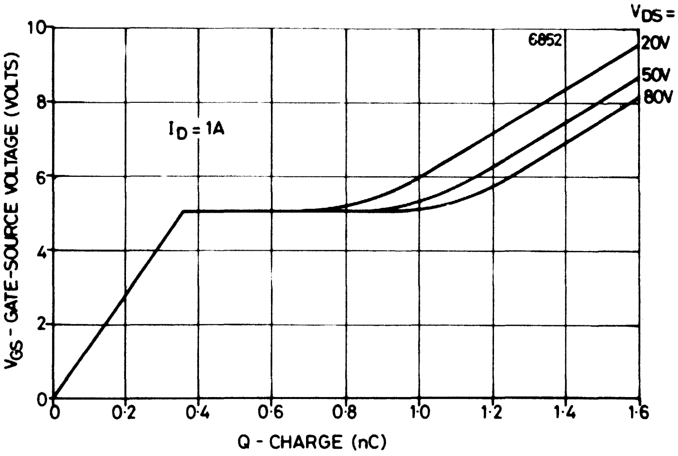


Fig. 10 Typical gate charge v gate-source voltage

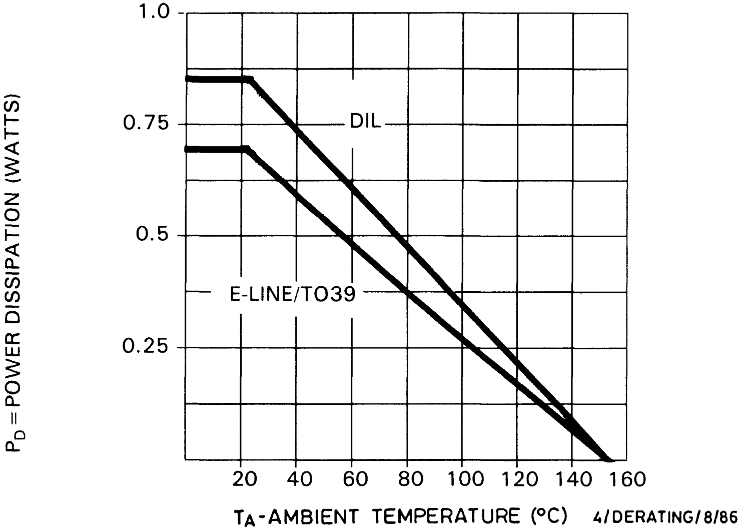


Fig. 11 Power v temperature derating curve (ambient)

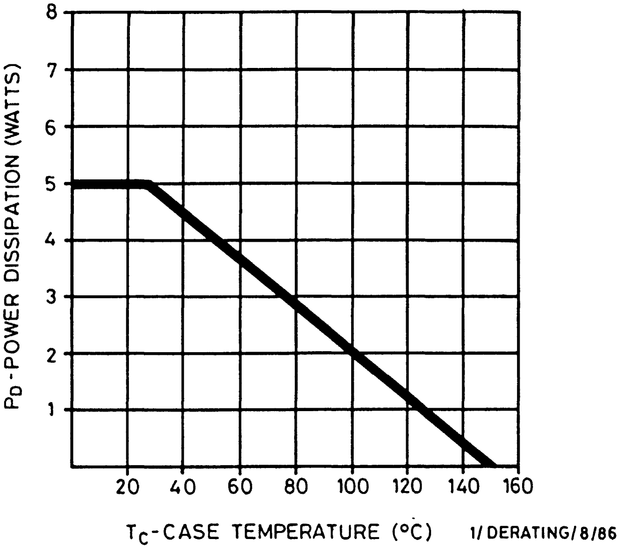


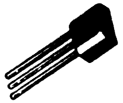
Fig. 12 Power v temperature derating curve (case)

N-channel enhancement mode vertical DMOS FET

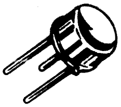
ZVN2120

FEATURES

- **Compact geometry**
- **Fast switching speeds**
- **No secondary breakdown**
- **Excellent temperature stability**
- **High input impedance**
- **Low current drive**
- **Ease of paralleling**



E-LINE (TO-92)
SUFFIX A or C



TO-39
SUFFIX B

DESCRIPTION

A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN2120A	200V	0.18A	10Ω
ZVN2120B	200V	0.46A	10Ω
ZVN2120C	200V	0.18A	10Ω

ZVN2120

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	TO-39	Unit
V_{DS}	Drain-source voltage	200	200	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.18	0.18	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	0.46	A
I_{DM}	Pulsed drain current	2	2	A
V_{GS}	Gate-source voltage	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	0.7	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	200	–	V	$I_D = 1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	1	3	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	10	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	100	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ ($T = 125°C$) (2)
$I_{D(on)}$	On-state drain current (1)	500	–	mA	$V_{DS} = 25V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	10	Ω	$I_D = 250mA$, $V_{GS} = 10V$
g_{fs}	Forward transconductance (1) (2)	100	–	mS	$V_{DS} = 25V$, $I_D = 250mA$
C_{iss}	Input capacitance (2)	–	85	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ $f = 1MHz$
C_{oss}	Common source output capacitance (2)	–	20	pF	
C_{rss}	Reverse transfer capacitance (2)	–	7	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	8	ns	$V_{DD} \approx 25V$, $I_D = 250mA$
t_r	Rise time (2) (3)	–	8	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	20	ns	
t_f	Fall time (2) (3)	–	12	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.

(2) Sample test.

(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

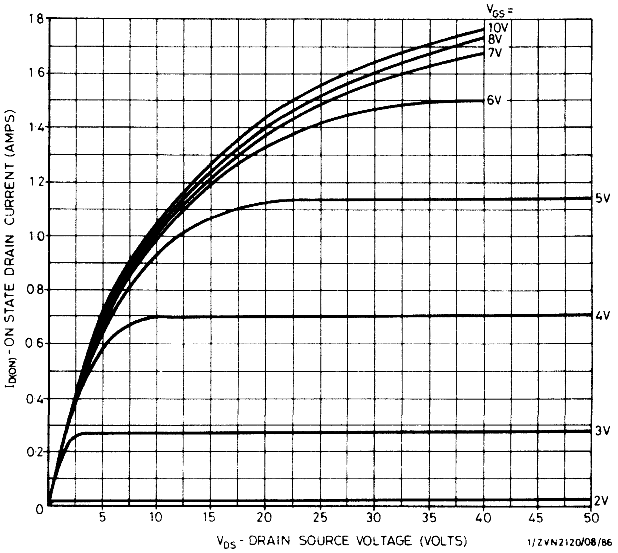


Fig. 1 Typical output characteristics

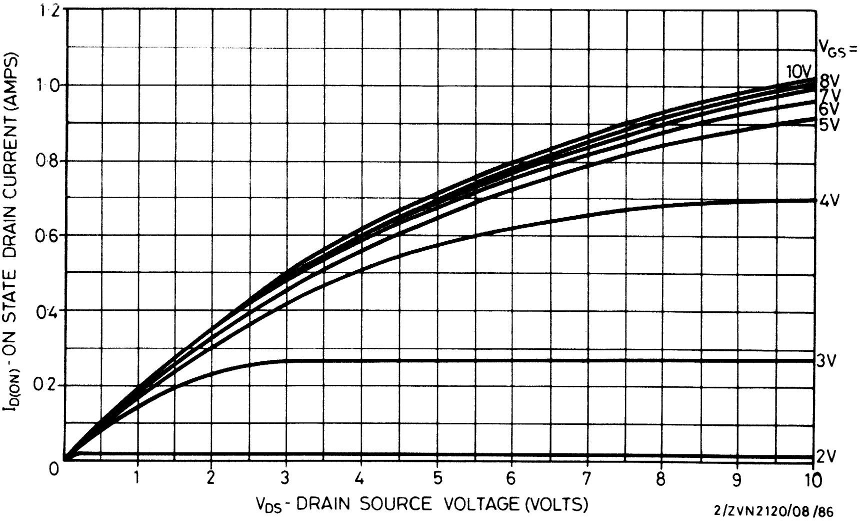


Fig. 2 Typical saturation characteristics

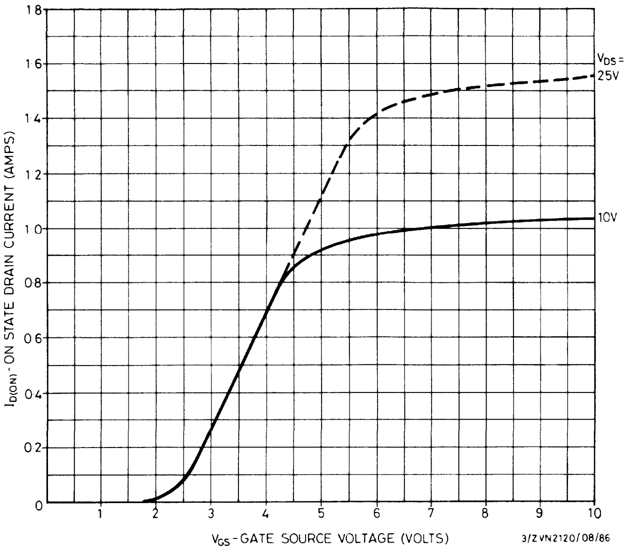


Fig. 3 Typical transfer characteristics

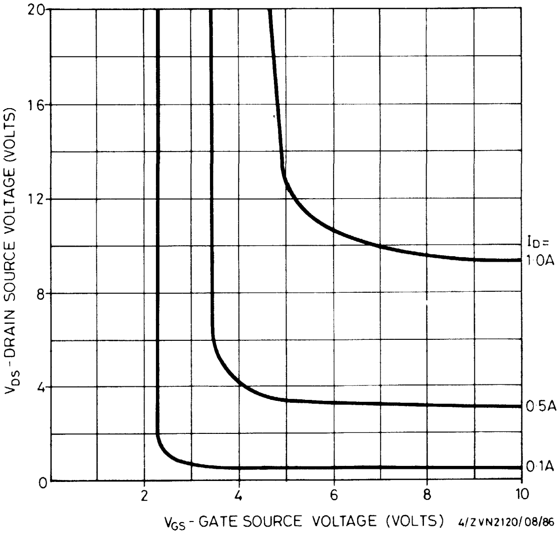


Fig. 4 Typical voltage saturation characteristics

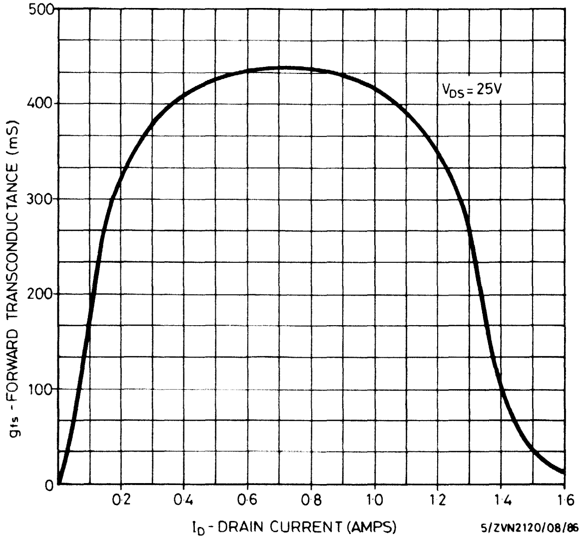


Fig. 5 Typical transconductance v drain current

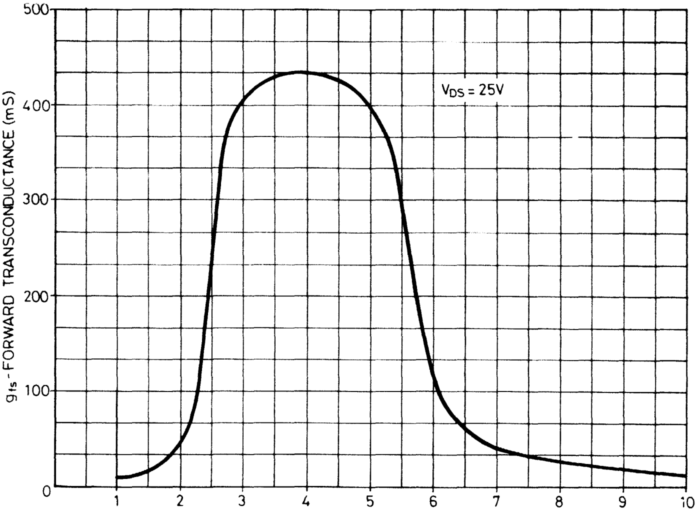


Fig. 6 Typical transconductance v gate-source voltage

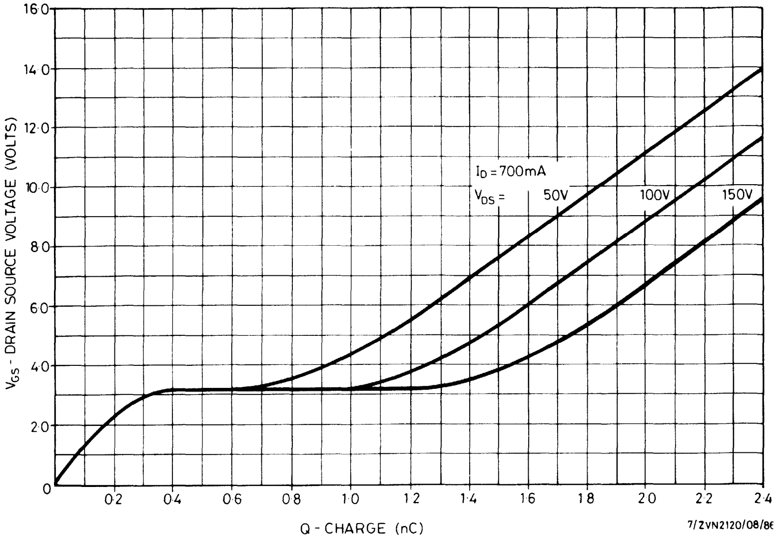


Fig. 7 Typical gate charge v gate-source voltage

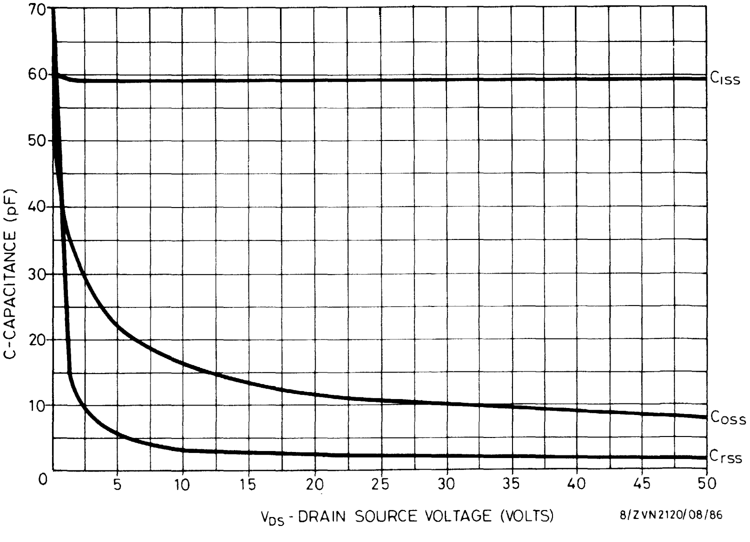


Fig. 8 Typical capacitance v drain-source voltage

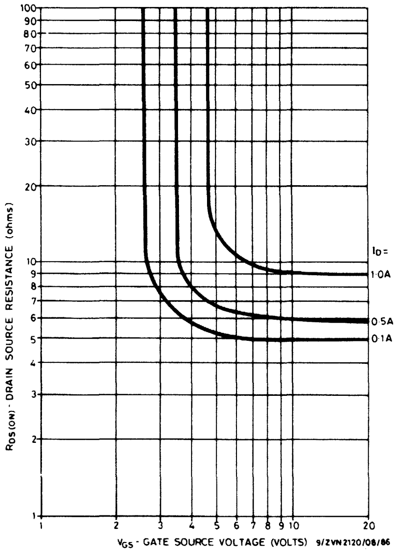


Fig. 9 Typical on-resistance v gate-source voltage

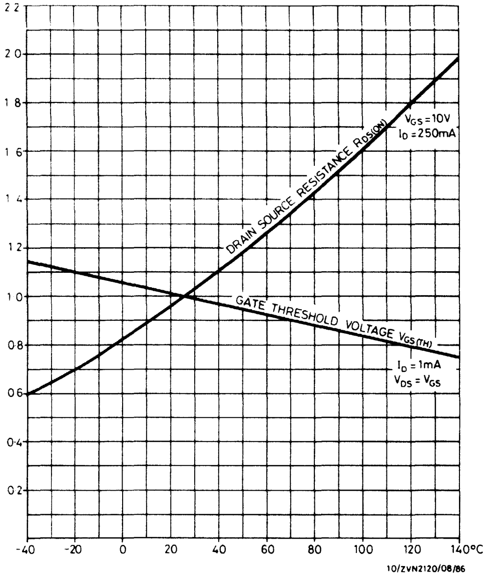


Fig. 10 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

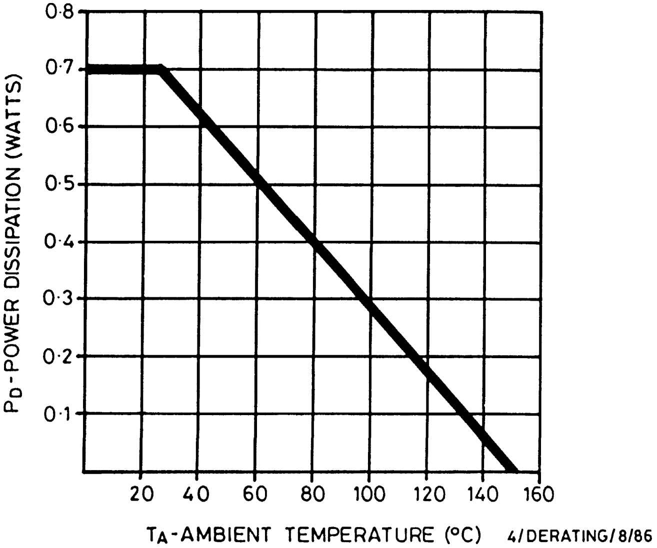


Fig. 11 Power v temperature derating curve (ambient)

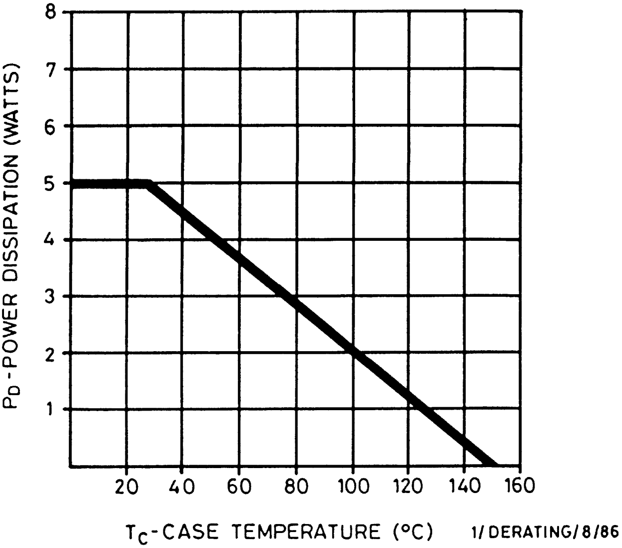


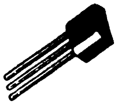
Fig. 12 Power v temperature derating curve (case)

N-channel enhancement mode vertical DMOS FET

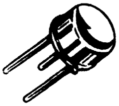
ZVN2535

FEATURES

- **Compact geometry**
- **Fast switching speeds**
- **No secondary breakdown**
- **Excellent temperature stability**
- **High input impedance**
- **Low current drive**
- **Ease of paralleling**



E-LINE (TO-92)
SUFFIX A



TO-39
SUFFIX B

DESCRIPTION

A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN2535A	350V	0.09A	35Ω
ZVN2535B	350V	0.25A	35Ω

ZVN2535

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	TO-39	Unit
V_{DS}	Drain-source voltage	350	350	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.09	0.09	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	0.25	A
I_{DM}	Pulsed drain current	1	1	A
V_{GS}	Gate-source voltage	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	0.7	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	350	–	V	$I_D = 1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	1	3	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate-body leakage	–	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	10	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	400	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	250	–	mA	$V_{DS} = 25V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	35	Ω	$I_D = 100mA$, $V_{GS} = 10V$
g_{fs}	Forward transconductance (1) (2)	100	–	mS	$V_{DS} = 25V$, $I_D = 100mA$
C_{iss}	Input capacitance (2)	–	70	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	10	pF	
C_{rss}	Reverse transfer capacitance (2)	–	4	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	7	ns	$V_{DD} \approx 25V$, $I_D = 100mA$
t_r	Rise time (2) (3)	–	7	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	16	ns	
t_f	Fall time (2) (3)	–	10	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽2%.

(2) Sample test.

(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

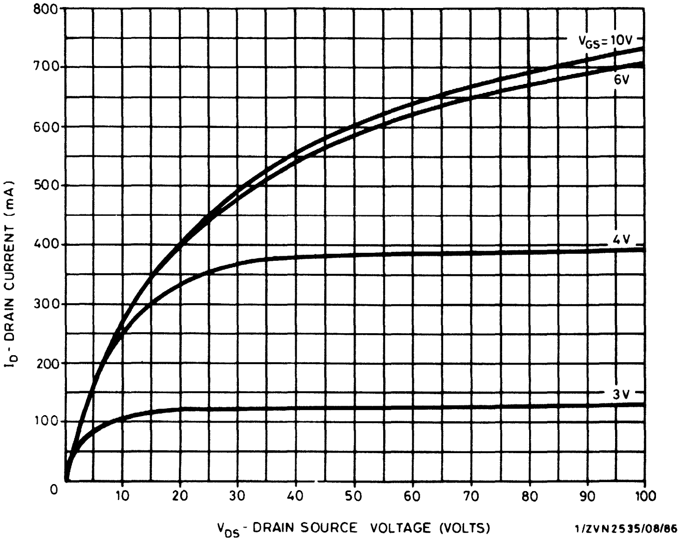


Fig. 1 Typical output characteristics

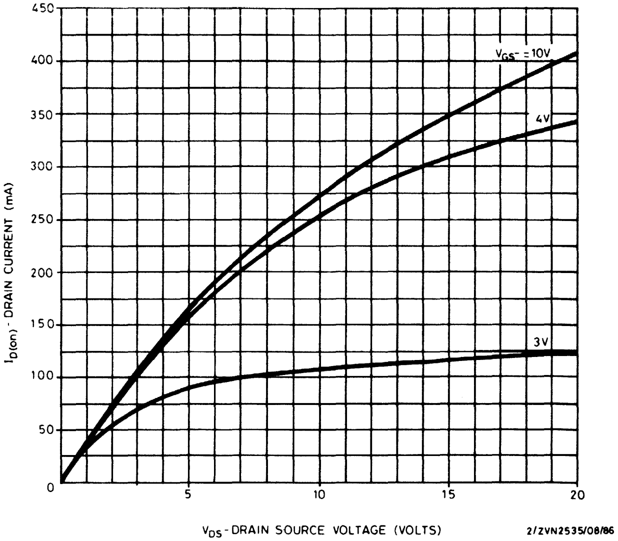


Fig. 2 Typical saturation characteristics

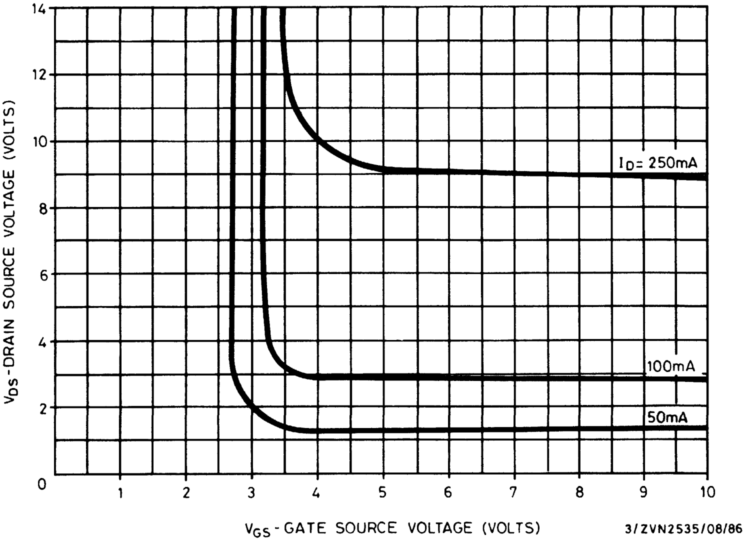


Fig. 3 Typical voltage saturation characteristics

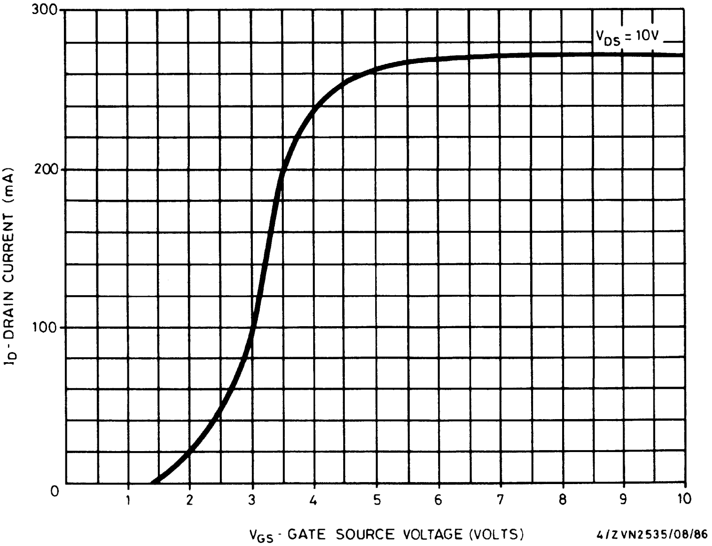


Fig. 4 Typical transfer characteristics

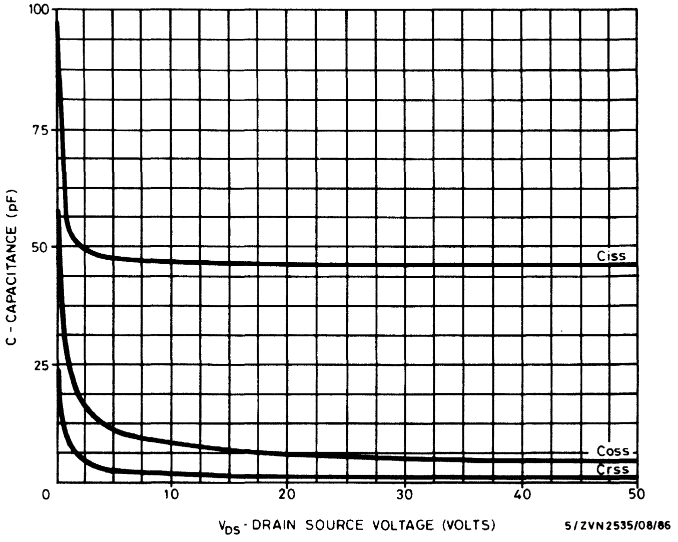


Fig. 5 Typical capacitance v drain-source voltage

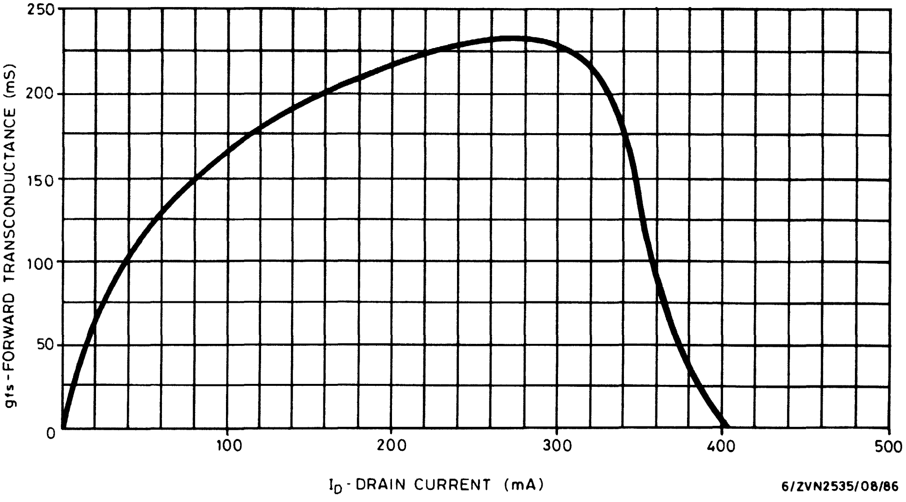


Fig. 6 Typical transconductance v drain current

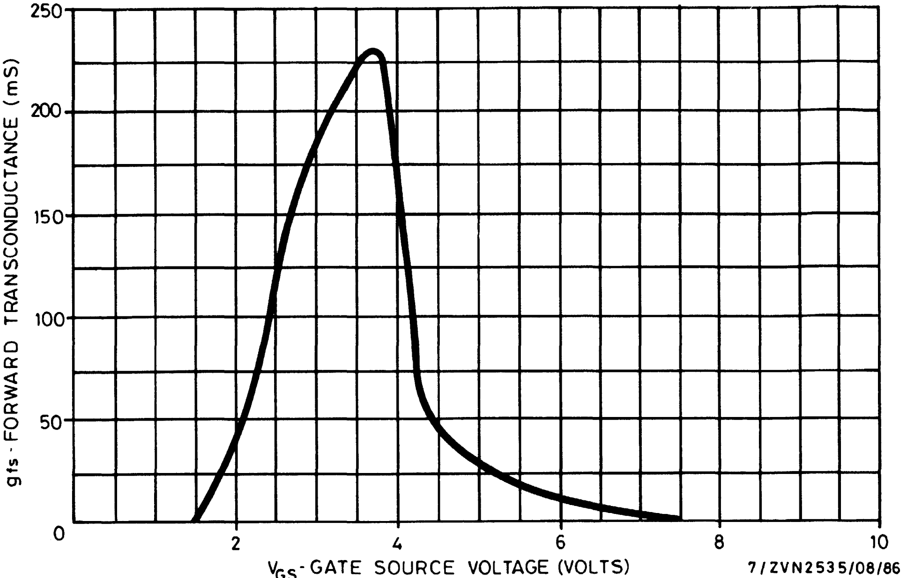


Fig. 7 Typical transconductance v gate-source voltage

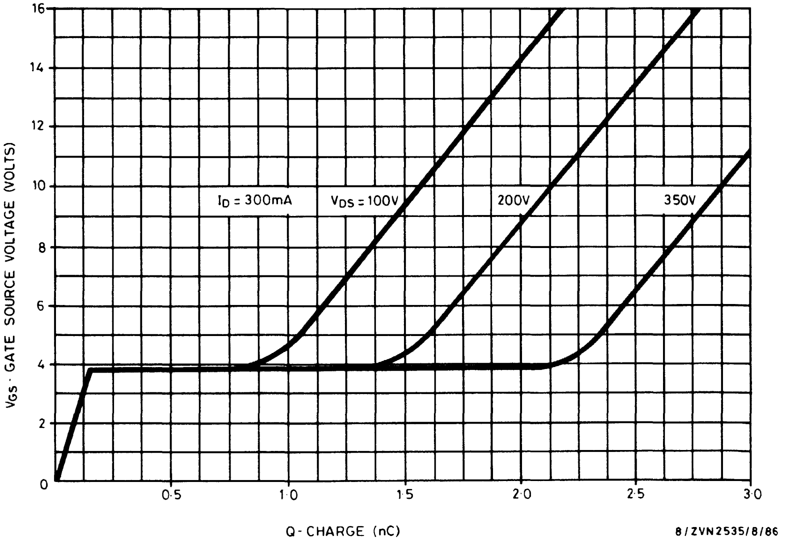


Fig. 8 Typical gate charge v gate-source voltage

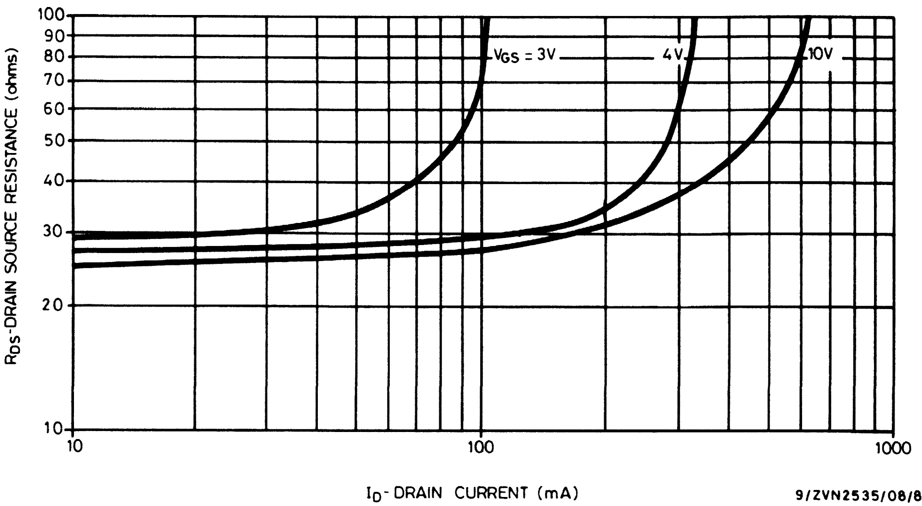


Fig. 9 Typical on-resistance v drain current

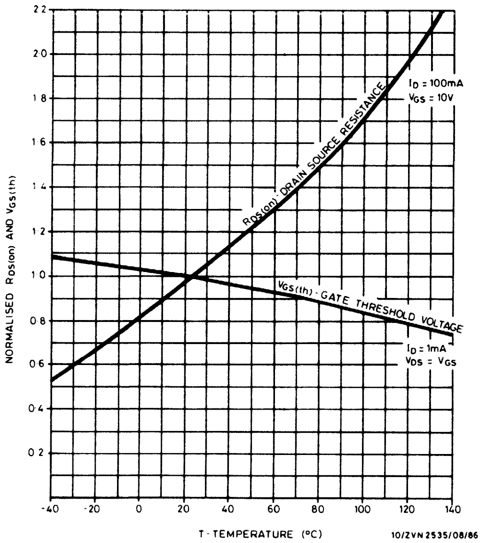


Fig. 10 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

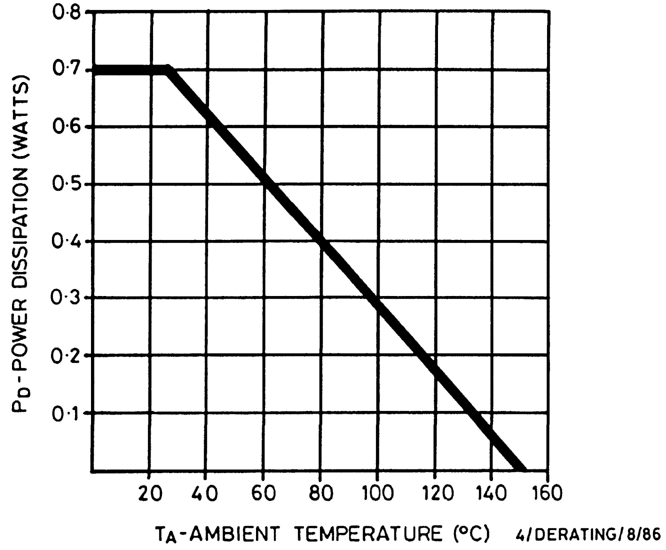


Fig. 11 Power v temperature derating curve (ambient)

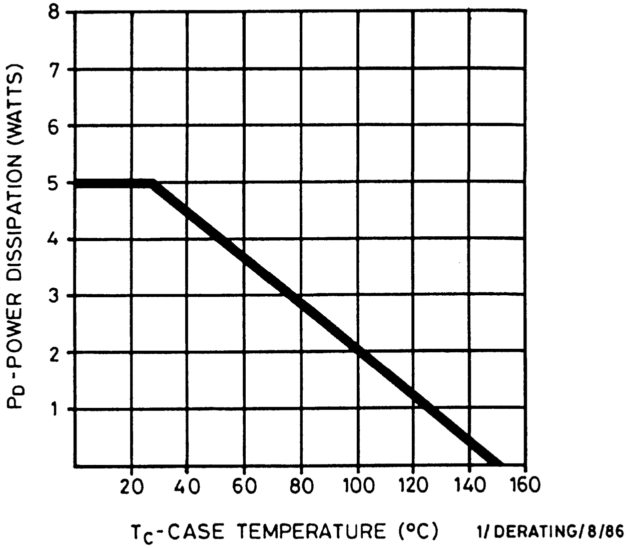


Fig. 12 Power v temperature derating curve (case)

N-Channel enhancement mode vertical DMOS FET

ZVN3306

FEATURES

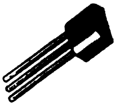
- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling

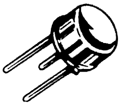
DESCRIPTION

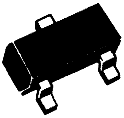
A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

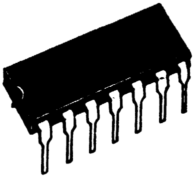
PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN3306A	60V	0.27A	5Ω
ZVN3306B	60V	0.75A	5Ω
ZVN3306F	60V	0.15A	5Ω
ZVN3306E	60V	0.27A	5Ω


E-LINE (TO-92)
SUFFIX A


TO-39
SUFFIX B


SOT-23
SUFFIX F


14 LEAD MOULDED DIL
SUFFIX E

ZVN3306

ABSOLUTE MAXIMUM RATINGS

	Parameters	E-line	TO-39	SOT-23	DIL	Units
V_{DS}	Drain-source voltage	60	60	60	60	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.27	0.27	0.15	0.27	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	0.75	–	–	A
I_{DM}	Pulsed drain current	3	3	3	3	A
V_{GS}	Gate-source voltage	±20	±20	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.625	0.625	0.25	0.85	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	–	–	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150				°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

	Parameter	Min.	Typ.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	60	–	–	V	$I_D = 1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	0.8	–	2.4	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	–	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	–	0.5	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	–	50	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	750	–	–	mA	$V_{DS} = 18V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	–	5	Ω	$I_D = 500mA$, $V_{GS} = 10V$
g_{fs}	Forward transconductance (1) (2)	150	–	–	mS	$V_{DS} = 18V$, $I_D = 500mA$
C_{iss}	Input capacitance (2)	–	–	35	pF	$V_{DS} = 18V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	–	25	pF	
C_{rss}	Reverse transfer capacitance (2)	–	–	8	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	3	5	ns	$V_{DD} \approx 18V$, $I_D = 500mA$
t_r	Rise time (2) (3)	–	4	7	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	4	6	ns	
t_f	Fall time (2) (3)	–	5	8	ns	

SOURCE-DRAIN DIODE CHARACTERISTICS

	Parameter	Typ.	Unit	Conditions
V_{SD}	Diode forward voltage (1)	0.85	V	$V_{GS}=0V$, $I_S=270mA$
t_{rr}	Reverse recovery time	90	ns	$V_{GS}=0V$, $I_F=270mA$ $I_R=100mA$

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽2%.

(2) Sample test.

(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

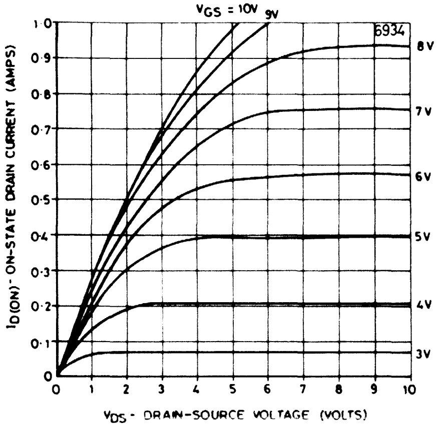


Fig. 1 Typical saturation characteristics

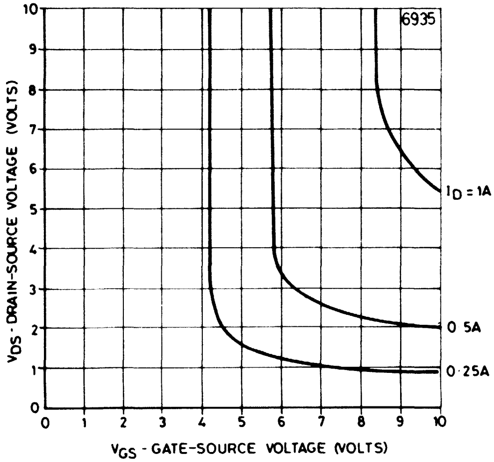


Fig. 2 Typical voltage saturation characteristics

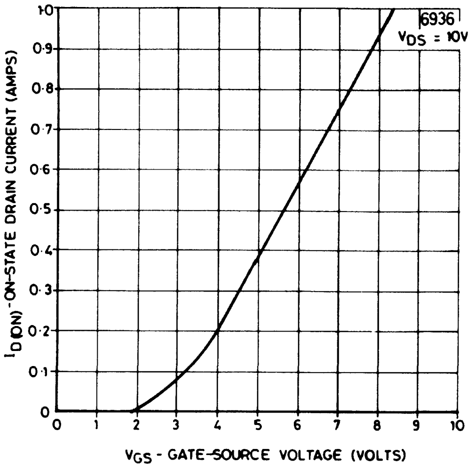


Fig. 3 Typical transfer characteristics

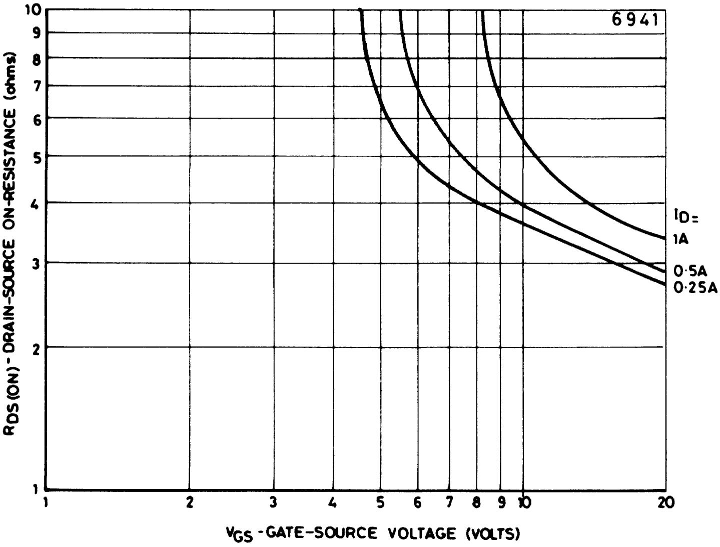


Fig. 4 Typical on-resistance v gate-source voltage

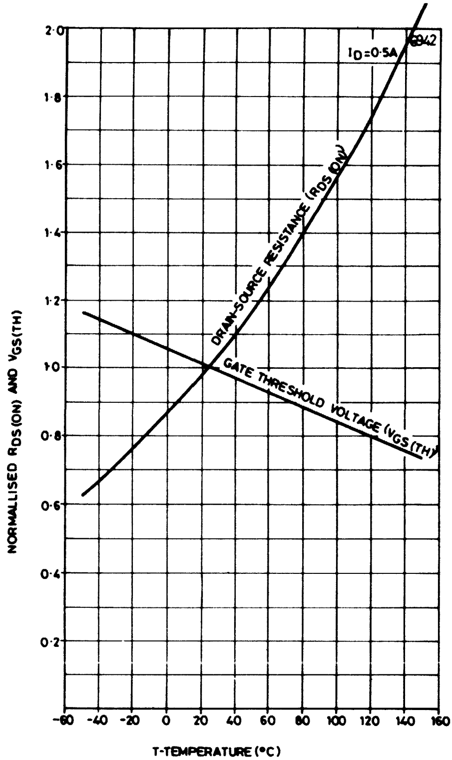


Fig. 5 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

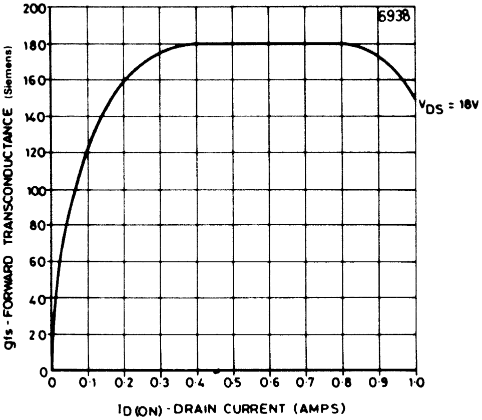


Fig. 6 Typical transconductance v drain current

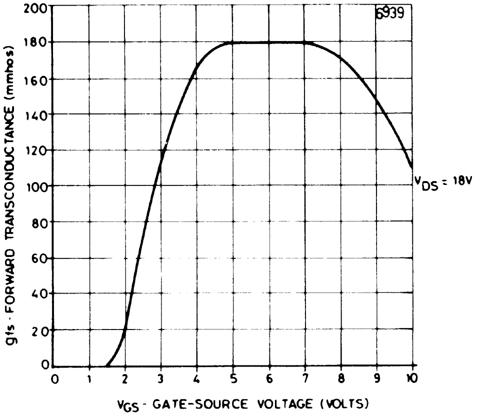


Fig. 7 Typical transconductance v gate-source voltage

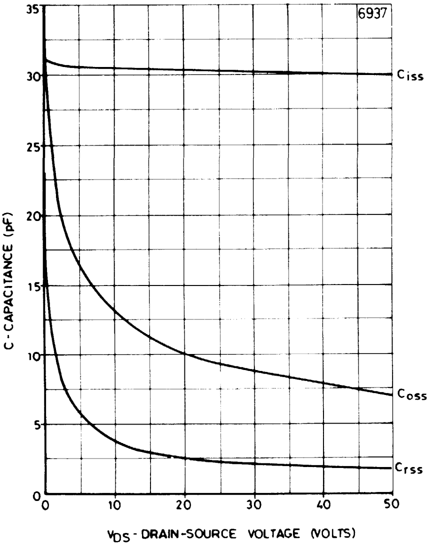


Fig. 8 Typical capacitance v drain-source voltage

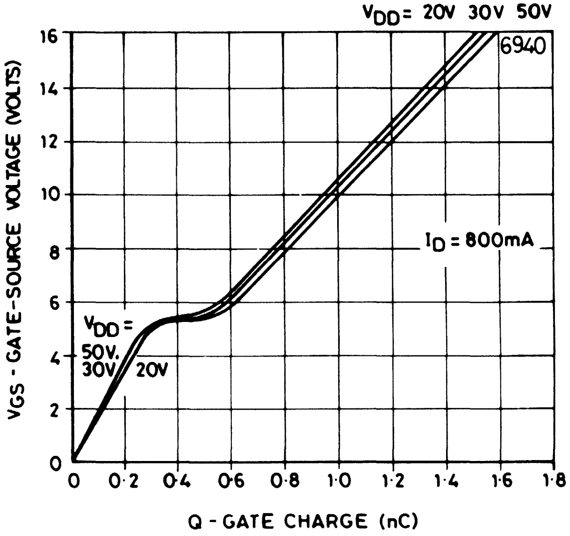


Fig. 9 Typical gate charge v gate-source voltage

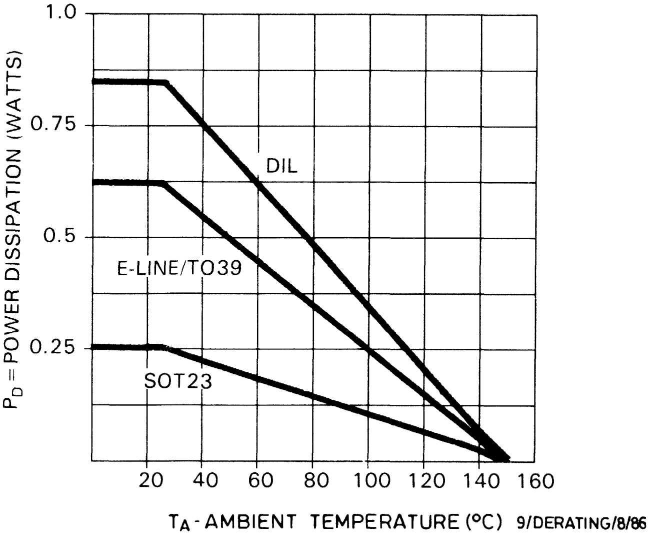


Fig. 10 Power v temperature derating curve (ambient)

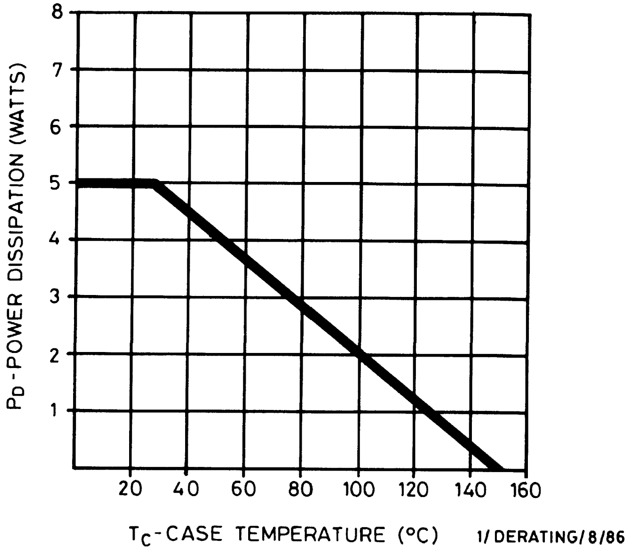


Fig. 11 Power v temperature derating curve (case)

N-channel enhancement mode vertical DMOS FET

ZVN3310

FEATURES

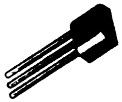
- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling

DESCRIPTION

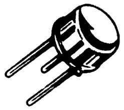
A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

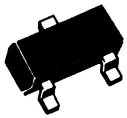
Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN3310A	100V	0.2A	10Ω
ZVN3310B	100V	0.5A	10Ω
ZVN3310F	100V	0.1A	10Ω



E-LINE (TO-92)
SUFFIX A



TO-39
SUFFIX B



SOT-23
SUFFIX F

ZVN3310

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	TO-39	SOT-23	Units
V_{DS}	Drain-source voltage	100	100	100	V
I_D	Continuous drain current (@ $T_A=25°C$)	0.2	0.2	0.1	A
I_D	Continuous drain current (@ $T_C=25°C$)	–	0.5	–	A
I_{DM}	Pulsed drain current	2	2	2	A
V_{GS}	Gate-source voltage	±20	±20	±20	V
P_D	Max. power dissipation (@ $T_A=25°C$)	0.625	0.625	0.25	W
P_D	Max. power dissipation (@ $T_C=25°C$)	–	5	–	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150			°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Typ.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	100	–	–	V	$I_D=1mA$, $V_{GS}=0V$
$V_{GS(th)}$	Gate-source threshold voltage	0.8	–	2.4	V	$I_D=1mA$, $V_{DS}=V_{GS}$
I_{GSS}	Gate body leakage	–	–	20	nA	$V_{GS}=\pm 20V$, $V_{DS}=0V$
I_{DSS}	Zero gate voltage drain current	–	–	1	μA	V_{DS} = Max. rating, $V_{GS}=0V$
		–	–	50	μA	$V_{DS}=0.8\times$ Max. rating $V_{GS}=0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	500	–	–	mA	$V_{DS}=25V$, $V_{GS}=10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	–	10	Ω	$I_D=500mA$, $V_{GS}=10V$
g_{fs}	Forward transconductance (1) (2)	100	–	–	mS	$V_{DS}=25V$, $I_D=500mA$
C_{iss}	Input capacitance (2)	–	–	40	pF	$V_{DS}=25V$, $V_{GS}=0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	–	15	pF	
C_{rss}	Reverse transfer capacitance (2)	–	–	5	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	3	5	ns	$V_{DD}\approx 25V$, $I_D=500mA$
t_r	Rise time (2) (3)	–	5	7	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	4	6	ns	
t_f	Fall time (2) (3)	–	5	7	ns	

SOURCE-DRAIN DIODE CHARACTERISTICS

	Parameter	Typ.	Unit	Conditions
V_{SD}	Diode forward voltage (1)	0.82	V	$V_{GS}=0V$, $I_S=200mA$

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽2%.

(2) Sample test.

(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

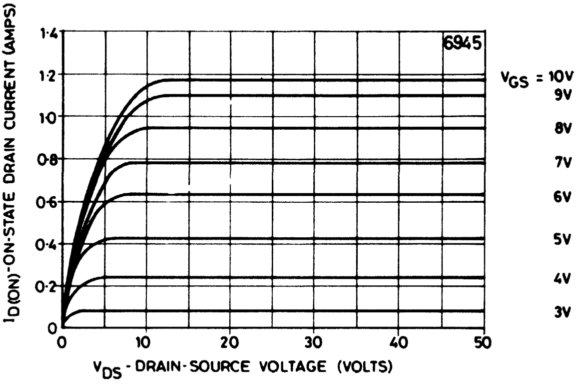


Fig. 1 Typical output characteristics

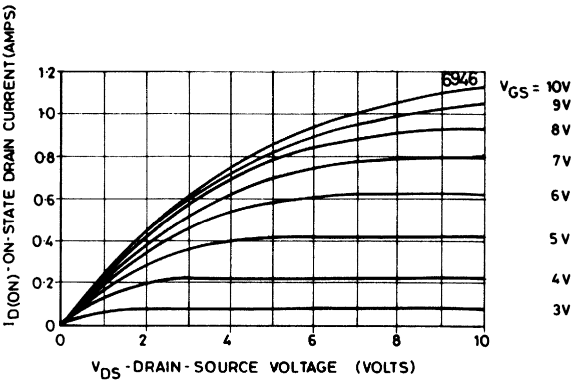


Fig. 2 Typical saturation characteristics

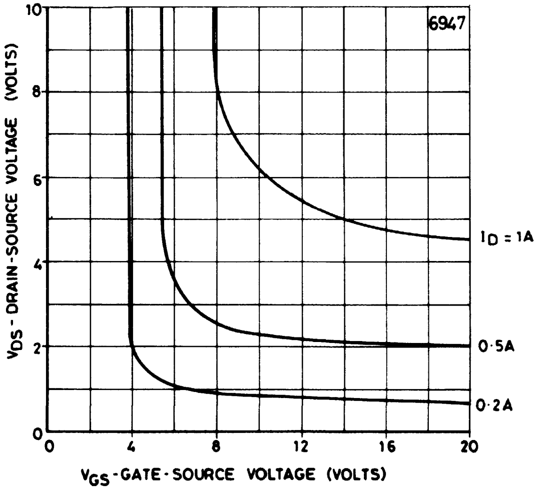


Fig. 3 Typical voltage saturation characteristics

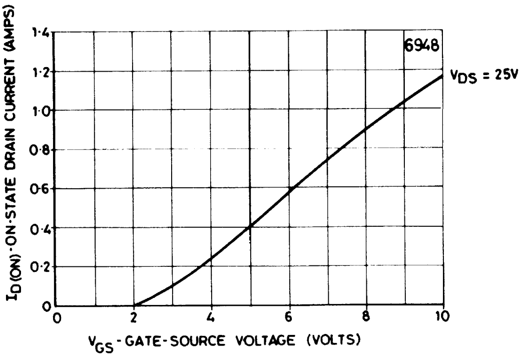


Fig. 4 Typical transfer characteristics

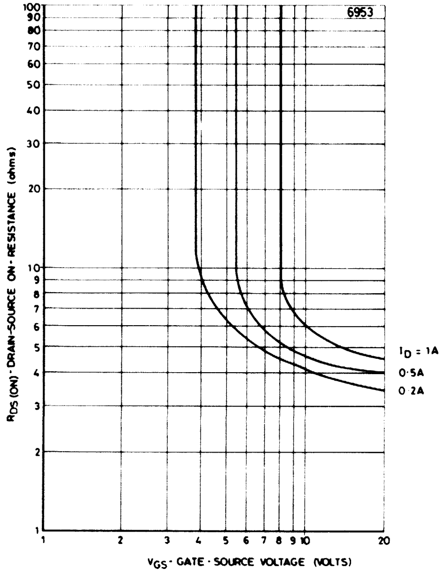


Fig. 5 Typical on-resistance v gate-source voltage

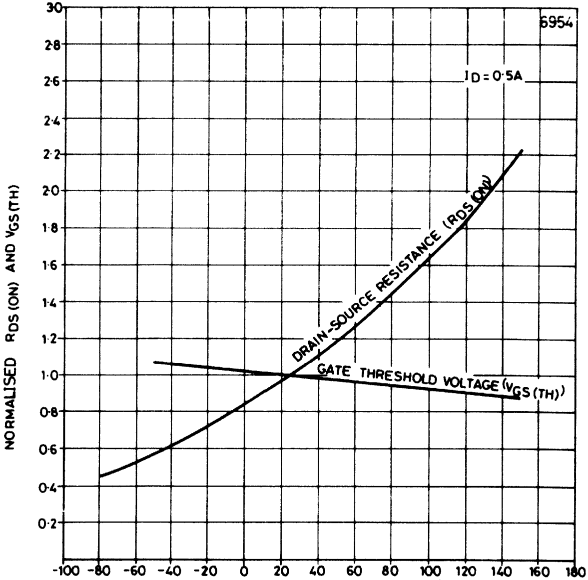


Fig. 6 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

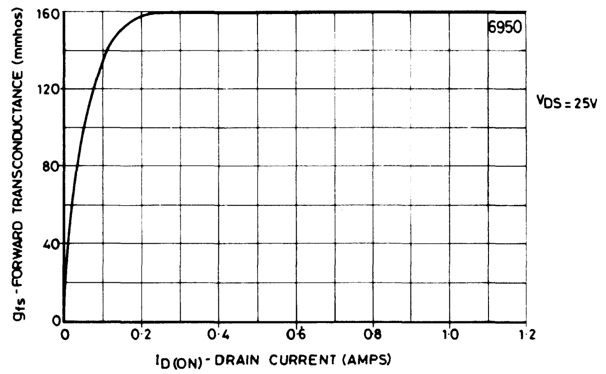


Fig. 7 Typical transconductance v drain current

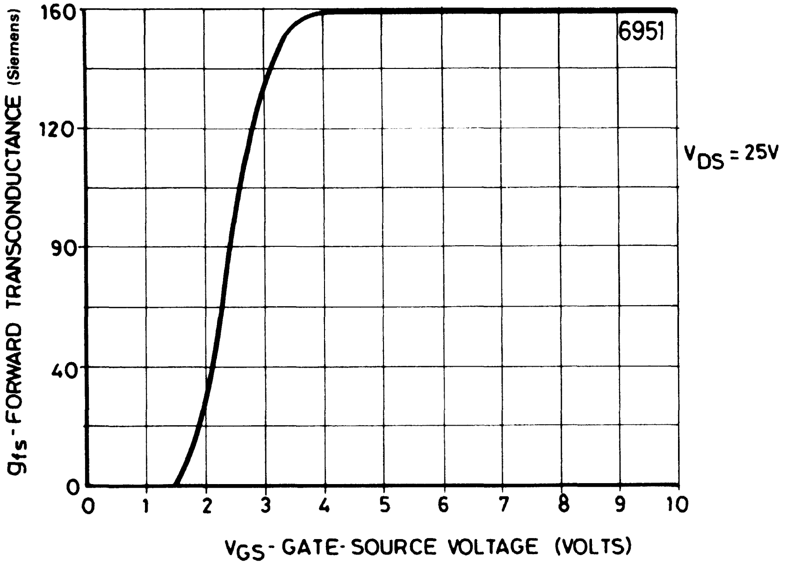


Fig. 8 Typical transconductance v gate-source voltage

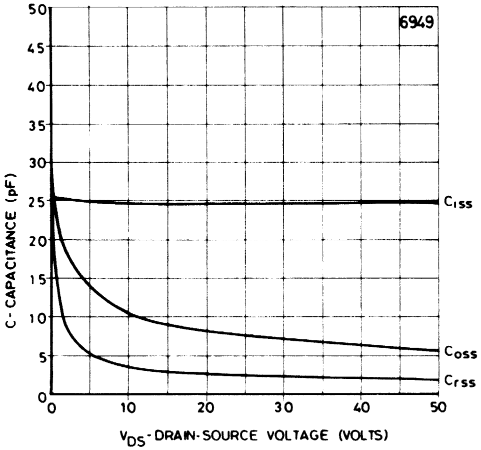


Fig. 9 Typical capacitance v drain-source voltage

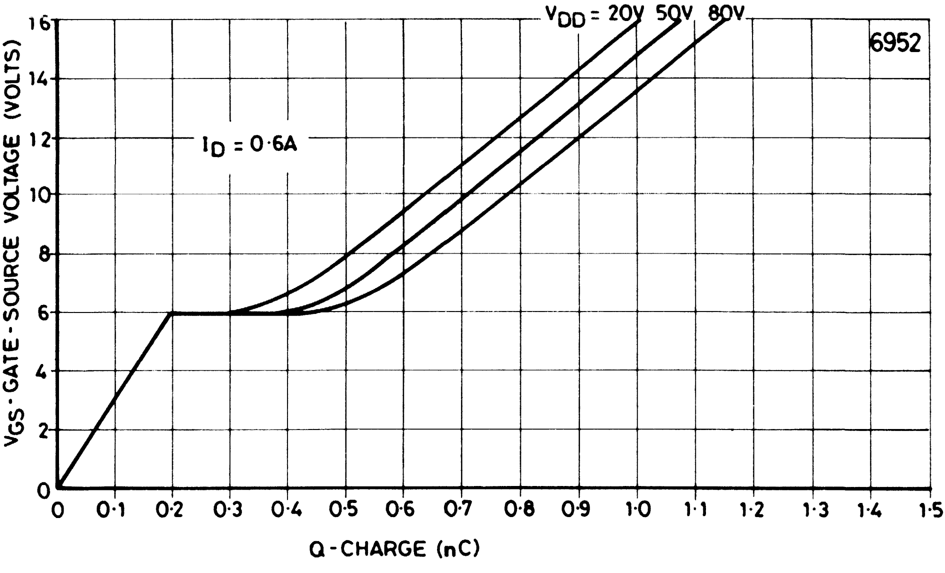


Fig. 10 Typical gate charge v gate-source voltage

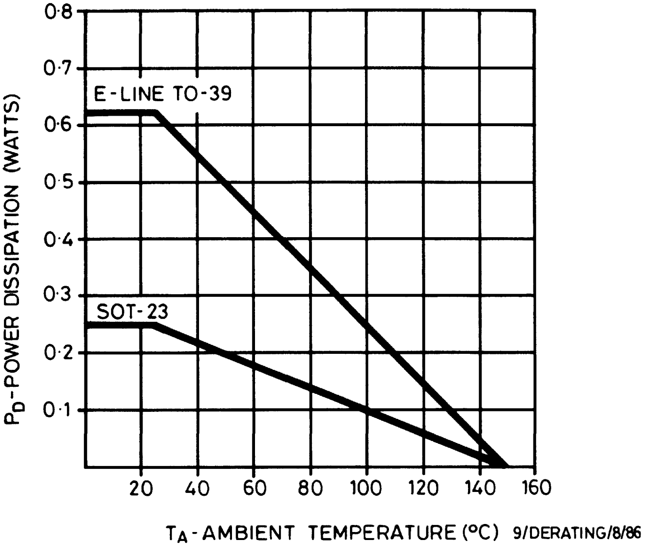


Fig. 11 Power v temperature derating curve (ambient)

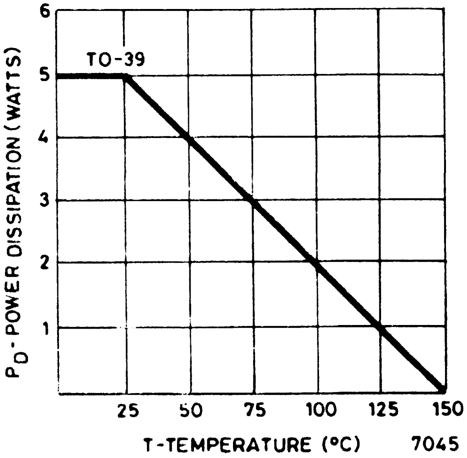


Fig. 12 Power v temperature derating curve (case)

N-channel enhancement mode vertical DMOS FET

ZVN3320

FEATURES

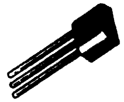
- **Compact geometry**
- **Fast switching speeds**
- **No secondary breakdown**
- **Excellent temperature stability**
- **High input impedance**
- **Low current drive**
- **Ease of paralleling**

DESCRIPTION

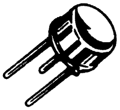
A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

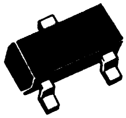
Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN3320A	200V	0.1 A	25Ω
ZVN3320B	200V	0.25 A	25Ω
ZVN3320F	200V	0.06 A	25Ω



E-LINE (TO-92)
SUFFIX A



TO-39
SUFFIX B



SOT-23
SUFFIX F

ZVN3320

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	TO-39	SOT-23	Units
V_{DS}	Drain-source voltage	200	200	200	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.1	0.1	0.06	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	0.25	–	A
I_{DM}	Pulsed drain current	1	1	1	A
V_{GS}	Gate-source voltage	±20	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.625	0.625	0.25	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	–	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150			°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Typ.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	200	–	–	V	$I_D = 1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	1	–	3	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	0.1	100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	–	10	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	–	50	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ ($T = 125°C$) (2)
$I_{D(on)}$	On-state drain current (1)	250	–	–	mA	$V_{DS} = 25V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	–	25	Ω	$I_D = 100mA$, $V_{GS} = 10V$
g_{fs}	Forward transconductance (1) (2)	75	–	–	mS	$V_{DS} = 25V$, $I_D = 100mA$
C_{iss}	Input capacitance (2)	–	–	45	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	–	18	pF	
C_{rss}	Reverse transfer capacitance (2)	–	–	5	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	–	5	ns	$V_{DD} \approx 25V$, $I_D = 100mA$
t_r	Rise time (2) (3)	–	–	7	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	–	6	ns	
t_f	Fall time (2) (3)	–	–	6	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽2%.

(2) Sample test.

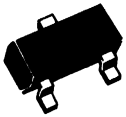
(3) Switching times measured with 50Ω source impedance and <5ns rise time on a pulse generator.

N-channel enhancement mode vertical DMOS FET

ZVN4106

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



SOT-23
SUFFIX F

DESCRIPTION

A compact cell geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN4106F	60V	0.2A	2.5Ω

ZVN4106

ABSOLUTE MAXIMUM RATINGS

Parameters		SOT-23	Unit
V_{DS}	Drain-source voltage	60	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.2	A
I_{DM}	Pulsed drain current	3	A
V_{GS}	Gate-source voltage	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.25	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	60	–	V	$I_D = 1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	1.3	3	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate-body leakage	–	100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	10	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	50	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	1	–	A	$V_{DS} = 25V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	2.5	Ω	$I_D = 500mA$, $V_{GS} = 10V$
		–	5	Ω	$I_D = 200mA$, $V_{GS} = 5V$
g_{fs}	Forward transconductance (1) (2)	150	–	mS	$V_{DS} = 25V$, $I_D = 500mA$
C_{iss}	Input capacitance (2)	–	35	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	25	pF	
C_{rss}	Reverse transfer capacitance (2)	–	8	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	5	ns	$V_{DD} \approx 25V$, $I_D = 500mA$
t_r	Rise time (2) (3)	–	7	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	6	ns	
t_f	Fall time (2) (3)	–	8	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽2%.

(2) Sample test.

(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

SOURCE - DRAIN DIODE CHARACTERISTICS

Parameter	Typ.	Unit	Conditions
V_{SD} Diode forward voltage (1)	0.79	V	$V_{GS}=0V$, $I_S=0.2A$
t_{rr} Reverse recovery time	70	ns	$V_{GS}=0V$, $I_F=0.2A$ $I_R=0.1A$

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.

(2) Sample test.

(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

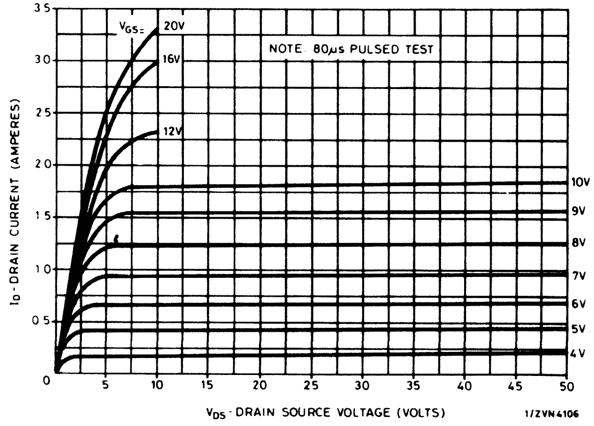


Fig. 1 Typical output characteristics

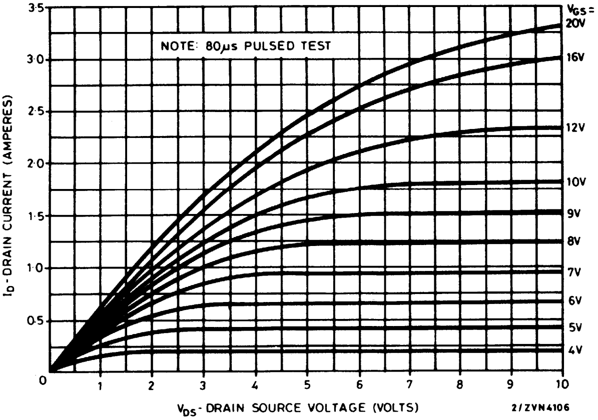


Fig. 2 Typical saturation characteristics

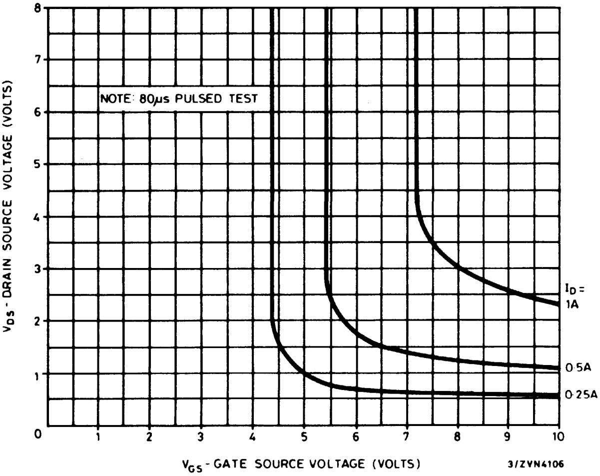


Fig. 3 Typical voltage saturation characteristics

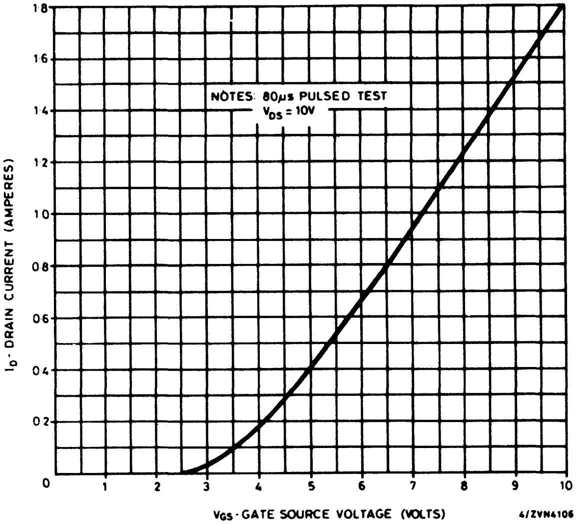


Fig. 4 Typical transfer characteristics

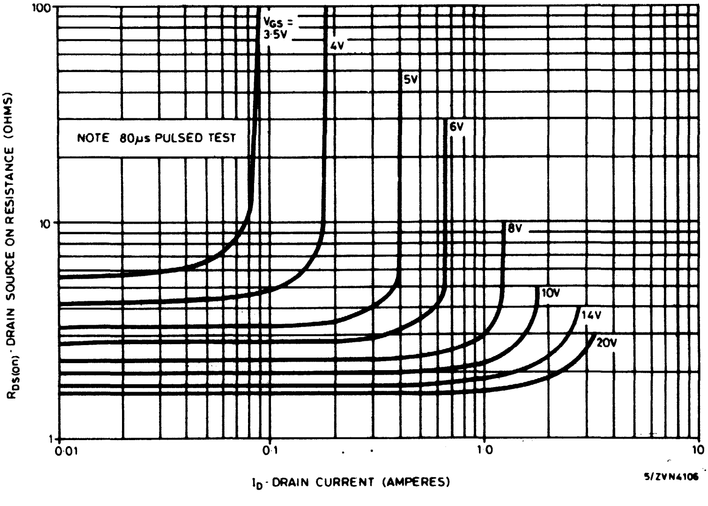


Fig. 5 Typical on-resistance v drain current

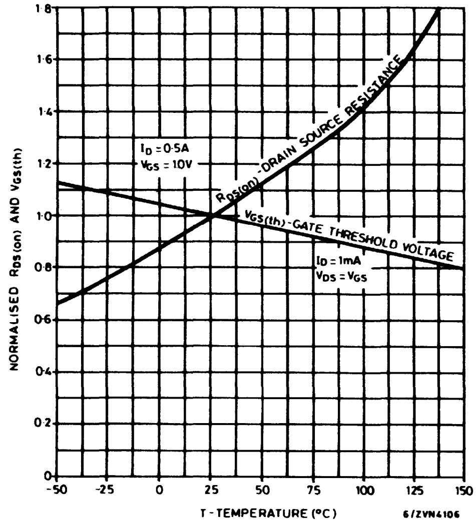


Fig. 6 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

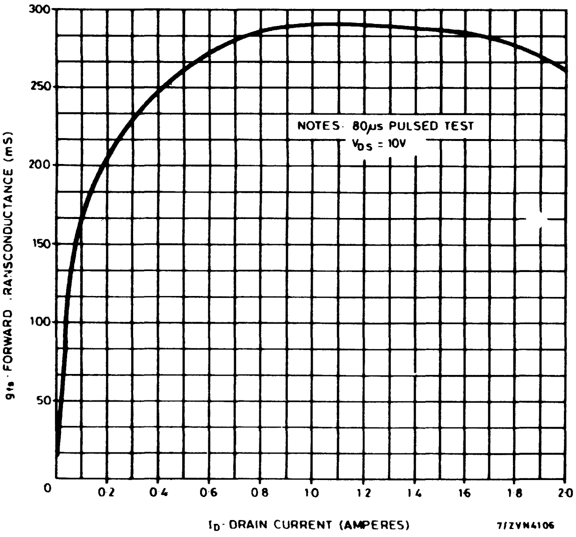


Fig. 7 Typical transconductance v drain current

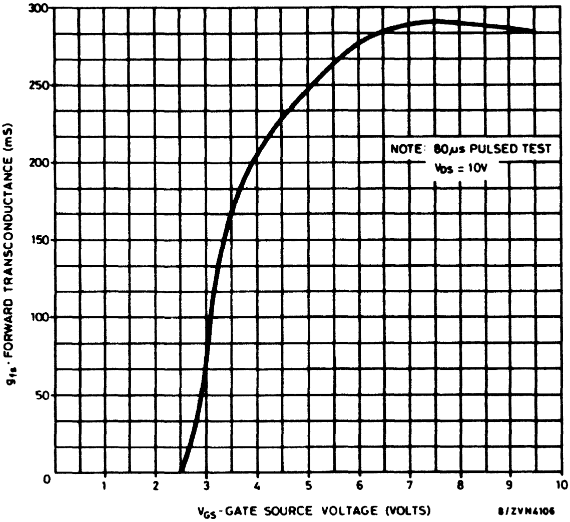


Fig. 8 Typical transconductance v gate-source voltage

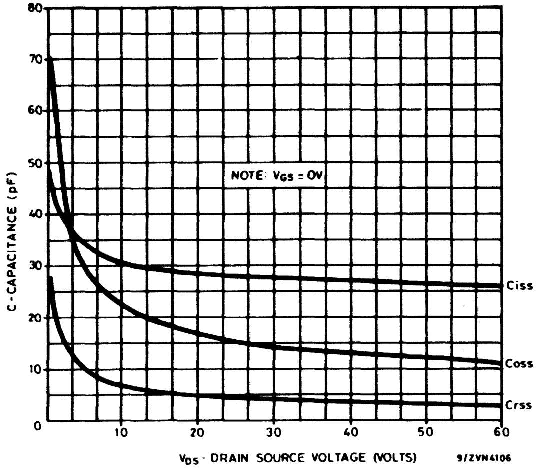


Fig. 9 Typical capacitance v drain-source voltage

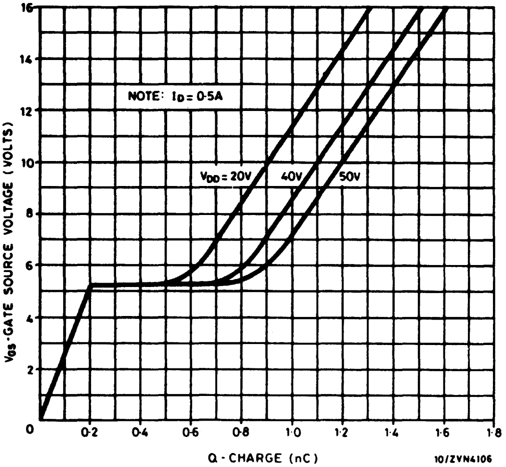


Fig. 10 Typical gate charge v gate-source voltage

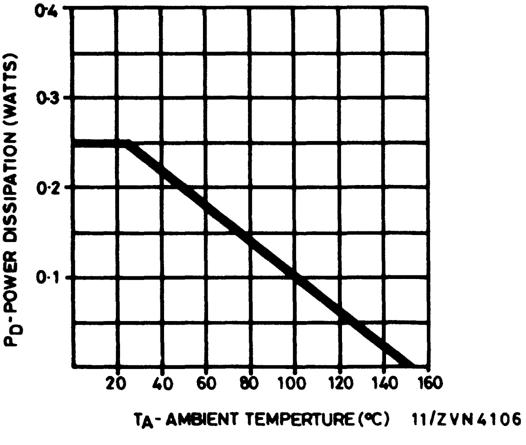


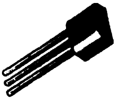
Fig. 11 Power v temperature derating curve (ambient)

N-channel enhancement mode vertical DMOS FET

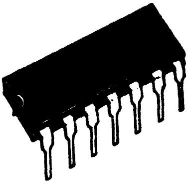
ZVN4206

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)
SUFFIX A or C



14 LEAD MOULDED DIL
SUFFIX E

DESCRIPTION

A compact cell geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN4206A	60V	0.6A	1Ω
ZVN4206C	60V	0.6A	1Ω
ZVN4206E	60V	0.6A	1Ω

ZVN4206

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	DIL	Unit
V_{DS}	Drain-source voltage	60	60	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.6	0.6	A
I_{DM}	Pulsed drain current	8	3	A
V_{GS}	Gate-source voltage	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	0.85	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	60	–	V	$I_D = 1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	1.3	3	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	10	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	100	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ ($T = 125°C$) (2)
$I_{D(on)}$	On-state drain current (1)	3	–	A	$V_{DS} = 25V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	1	Ω	$I_D = 1.5A$, $V_{GS} = 10V$
		–	1.5	Ω	$I_D = 0.5A$, $V_{GS} = 5V$
g_{fs}	Forward transconductance (1) (2)	0.3	–	S	$V_{DS} = 25V$, $I_D = 1.5A$
C_{iss}	Input capacitance (2)	–	100	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ $f = 1MHz$
C_{oss}	Common source output capacitance (2)	–	60	pF	
C_{rss}	Reverse transfer capacitance (2)	–	20	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	8	ns	$V_{DD} \approx 25V$, $I_D = 1.5A$
t_r	Rise time (2) (3)	–	12	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	12	ns	
t_f	Fall time (2) (3)	–	15	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ≤2%.

(2) Sample test.

(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

SOURCE - DRAIN DIODE CHARACTERISTICS

Parameter		Typ.	Unit	Conditions
V_{SD}	Diode forward voltage (1)	0.85	V	$V_{GS}=0V$, $I_S=0.6A$
t_{rr}	Reverse recovery time	70	ns	$V_{GS}=0V$, $I_F=0.6A$ $I_R=0.1A$

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.

(2) Sample test.

(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

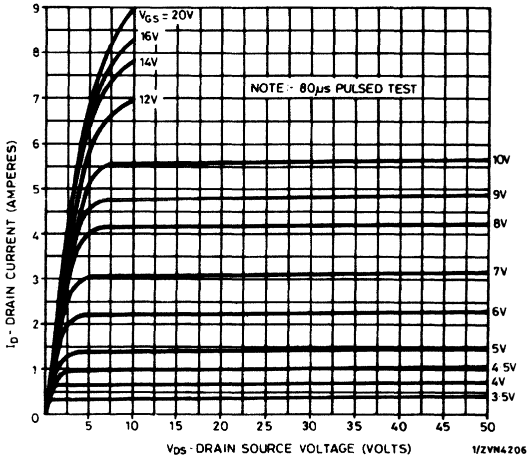


Fig. 1 Typical output characteristics

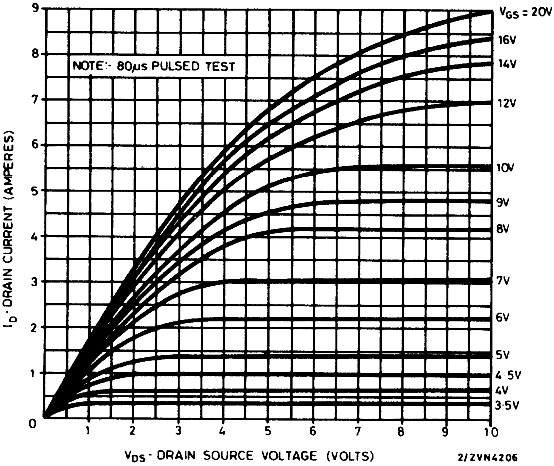


Fig. 2 Typical saturation characteristics

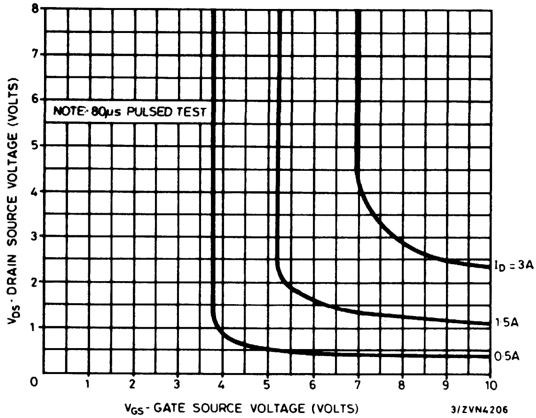


Fig. 3 Typical voltage saturation characteristics

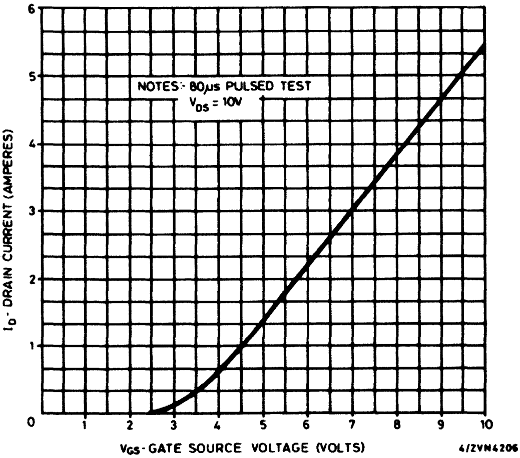


Fig. 4 Typical transfer characteristics

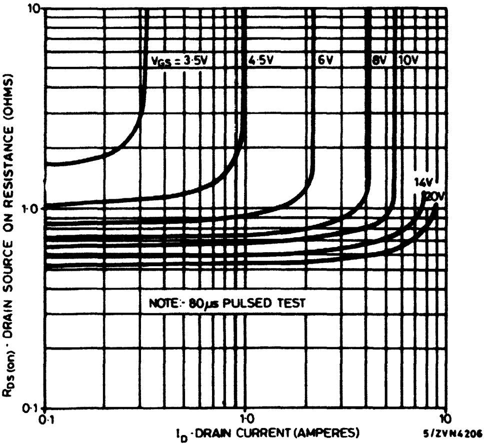


Fig. 5 Typical on-resistance v drain current

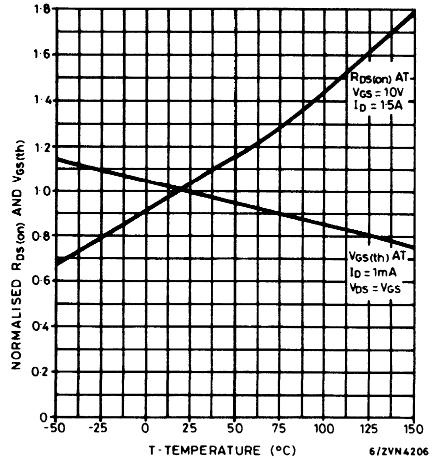


Fig. 6 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

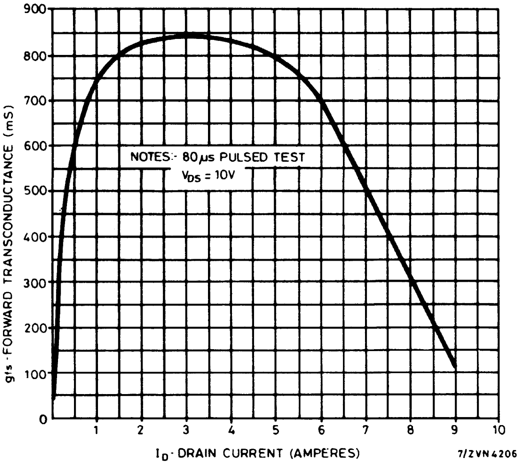


Fig. 7 Typical transconductance v drain current

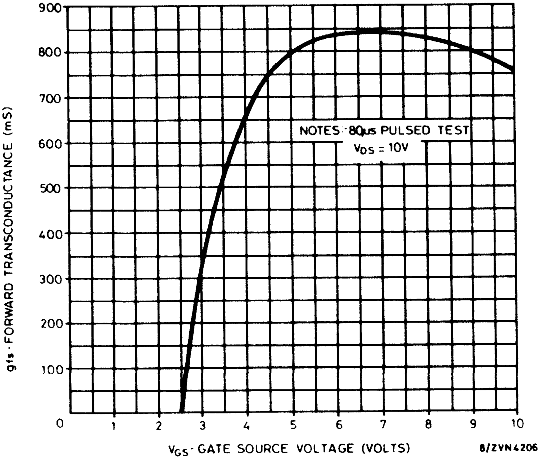


Fig. 8 Typical transconductance v gate-source voltage

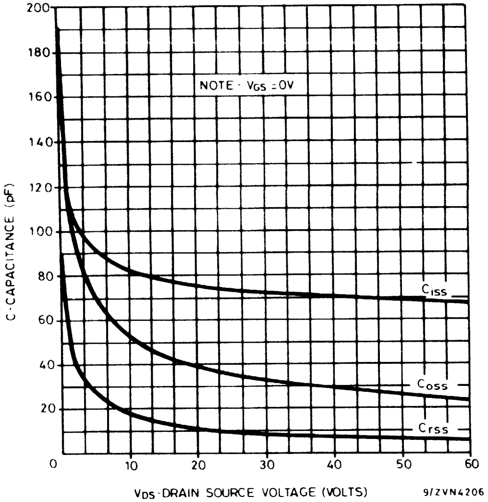


Fig. 9 Typical capacitance v drain-source voltage

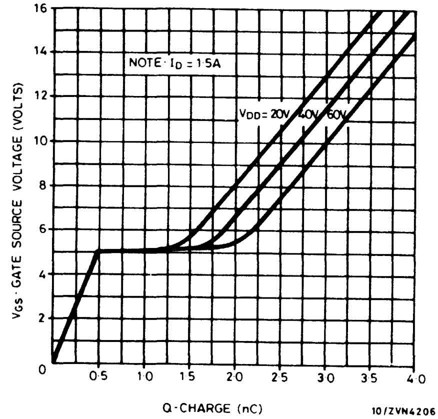


Fig. 10 Typical gate charge v gate-source voltage

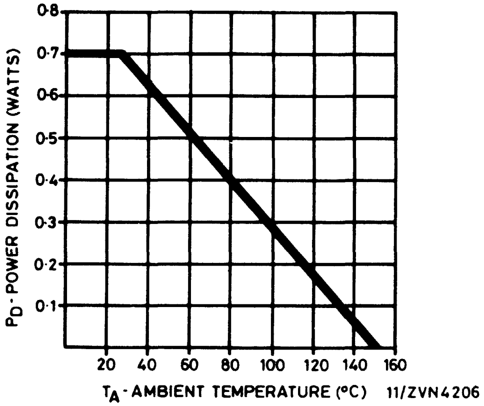


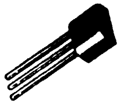
Fig. 11 Power v temperature derating curve (ambient)

P-channel enhancement mode vertical DMOS FET

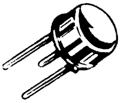
ZVP0120

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)
SUFFIX A



TO-39
SUFFIX B

DESCRIPTION

A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVP0120A	−200V	−0.11 A	32Ω
ZVP0120B	−200V	−0.25 A	32Ω

ZVP0120

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	TO-39	Unit
V_{DS}	Drain-source voltage	−200	−200	V
I_D	Continuous drain current (@ $T_A = 25°C$)	−0.11	−0.11	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	−0.25	A
I_{DM}	Pulsed drain current	−1	−1	A
V_{GS}	Gate-source voltage	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	0.7	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	−200	–	V	$I_D = -1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	−1.5	−3.5	V	$I_D = -1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	−10	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	−100	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	−250	–	mA	$V_{DS} = -25V$, $V_{GS} = -10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	32	Ω	$I_D = -125mA$, $V_{GS} = -10V$
g_{fs}	Forward transconductance (1) (2)	50	–	mS	$V_{DS} = -25V$, $I_D = -125mA$
C_{iss}	Input capacitance (2)	–	100	pF	$V_{DS} = -25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	25	pF	
C_{rss}	Reverse transfer capacitance (2)	–	7	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	7	ns	$V_{DD} \approx -25V$, $I_D = -125mA$
t_r	Rise time (2) (3)	–	15	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	12	ns	
t_f	Fall time (2) (3)	–	15	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ≤2%.

(2) Sample test.

(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

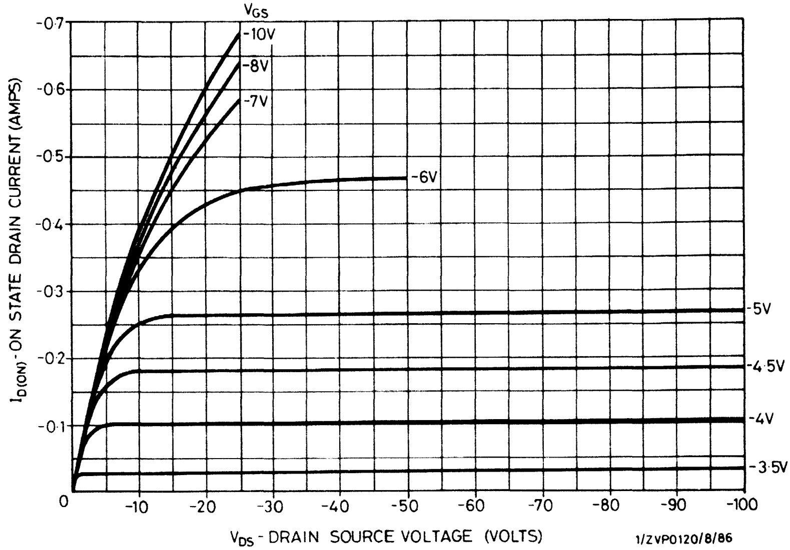


Fig. 1 Typical output characteristics

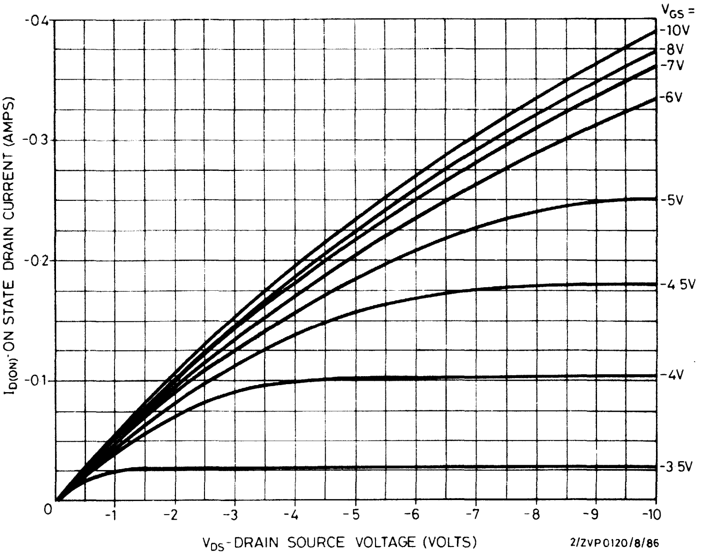


Fig. 2 Typical saturation characteristics

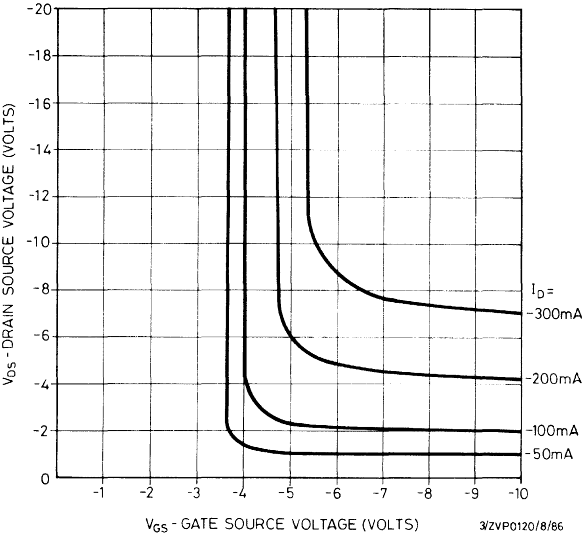


Fig. 3 Typical voltage saturation characteristics

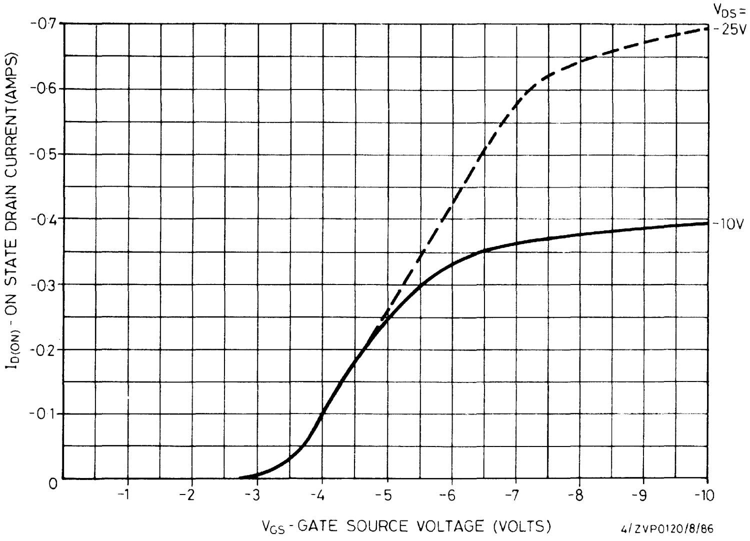


Fig. 4 Typical transfer characteristics

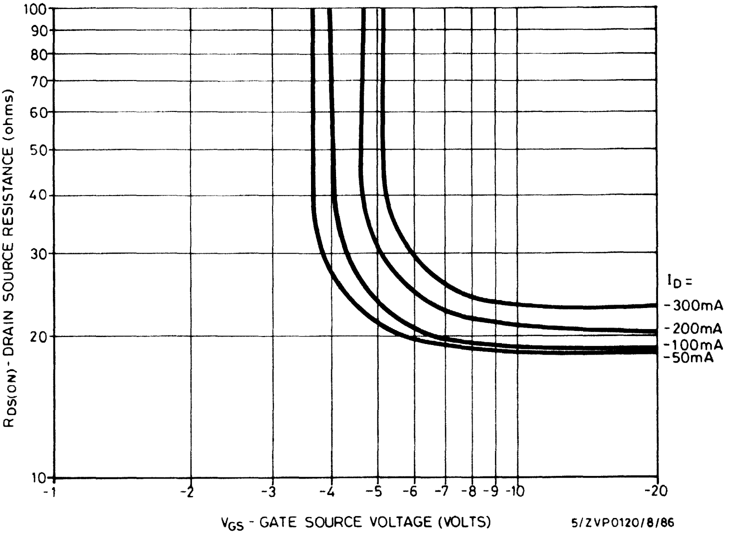


Fig. 5 Typical on-resistance v gate-source voltage

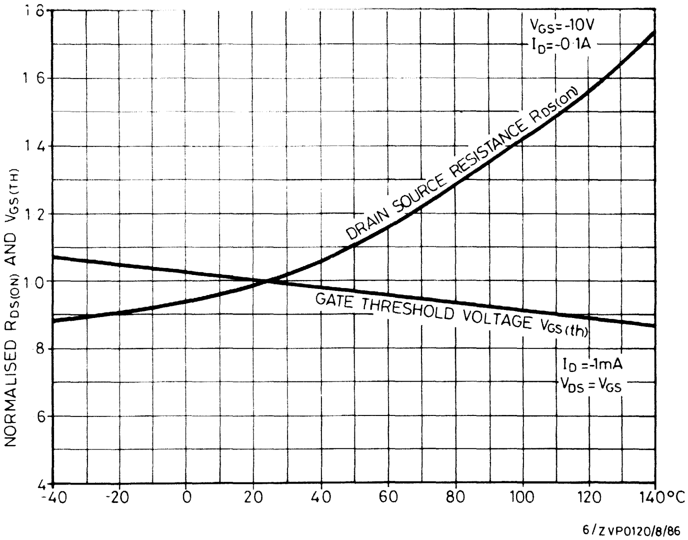


Fig. 6 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

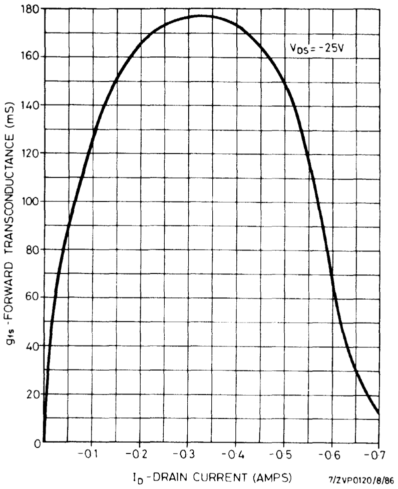


Fig. 7 Typical transconductance v drain current

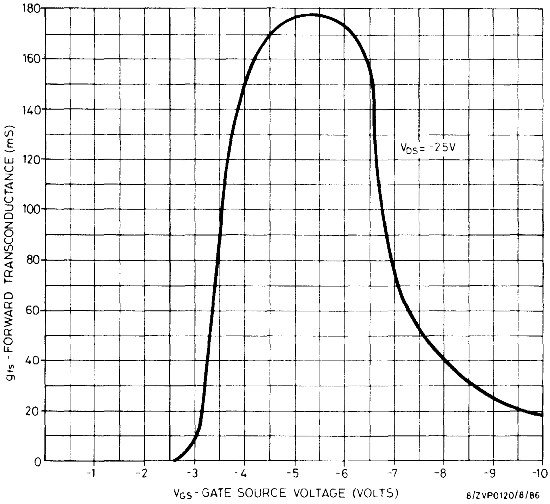


Fig. 8 Typical transconductance v gate-source voltage

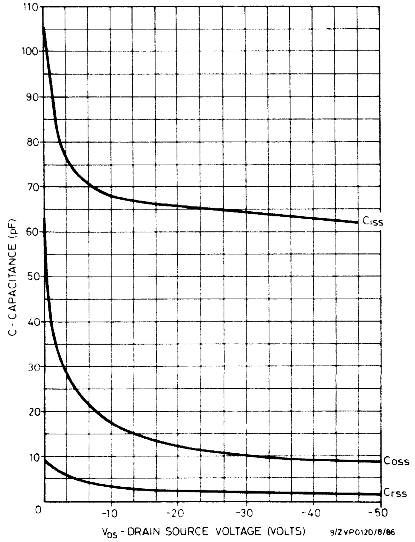


Fig. 9 Typical capacitance v drain-source voltage

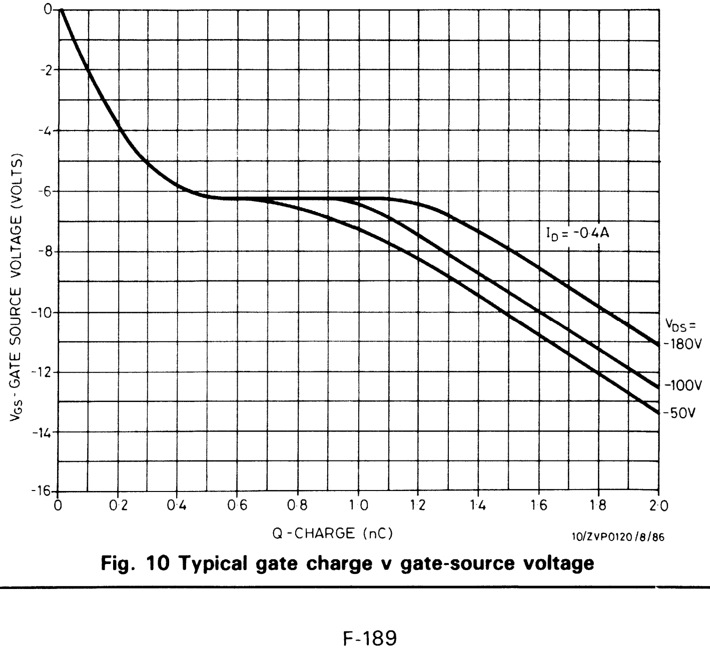


Fig. 10 Typical gate charge v gate-source voltage

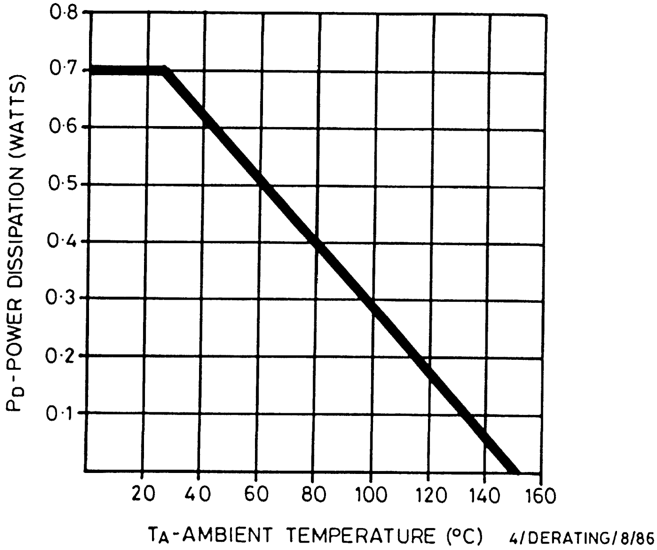


Fig. 11 Power v temperature derating curve (ambient)

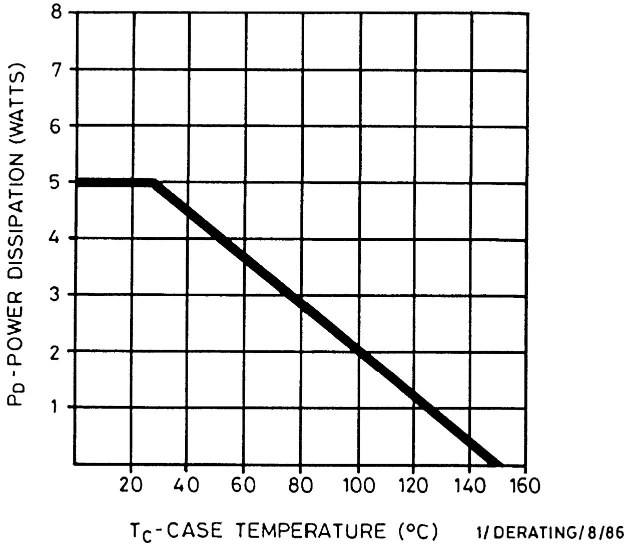


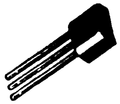
Fig. 12 Power v temperature derating curve (case)

P-channel enhancement mode vertical DMOS FET

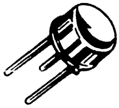
ZVP0535

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)
SUFFIX A



TO-39
SUFFIX B

DESCRIPTION

A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVP0535A	−350V	−0.05 A	100Ω
ZVP0535B	−350V	−0.12 A	100Ω

ZVP0535

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	TO-39	Unit
V_{DS}	Drain-source voltage	−350	−350	V
I_D	Continuous drain current (@ $T_A = 25°C$)	−0.05	−0.05	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	−0.12	A
I_{DM}	Pulsed drain current	−0.48	−0.48	A
V_{GS}	Gate-source voltage	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	0.7	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	−350	–	V	$I_D = -1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	−1.5	−4.5	V	$I_D = -1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate-body leakage	–	100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	−20	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	−2	mA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	−120	–	mA	$V_{DS} = -25V$, $V_{GS} = -10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	100	Ω	$I_D = -50mA$, $V_{GS} = -10V$
g_{fs}	Forward transconductance (1) (2)	40	–	mS	$V_{DS} = -25V$, $I_D = -50mA$
C_{iss}	Input capacitance (2)	–	120	pF	$V_{DS} = -25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	20	pF	
C_{rss}	Reverse transfer capacitance (2)	–	5	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	10	ns	$V_{DD} \approx -25V$, $I_D = -50mA$
t_r	Rise time (2) (3)	–	15	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	15	ns	
t_f	Fall time (2) (3)	–	20	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

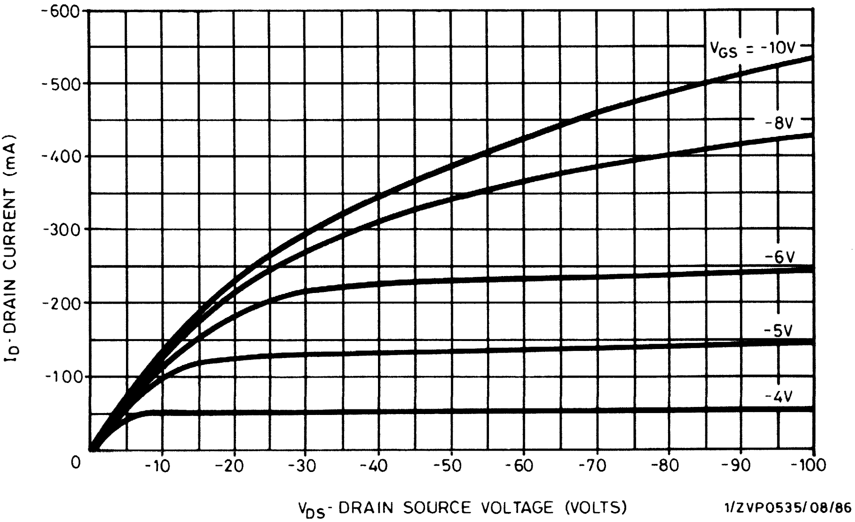


Fig. 1 Typical output characteristics

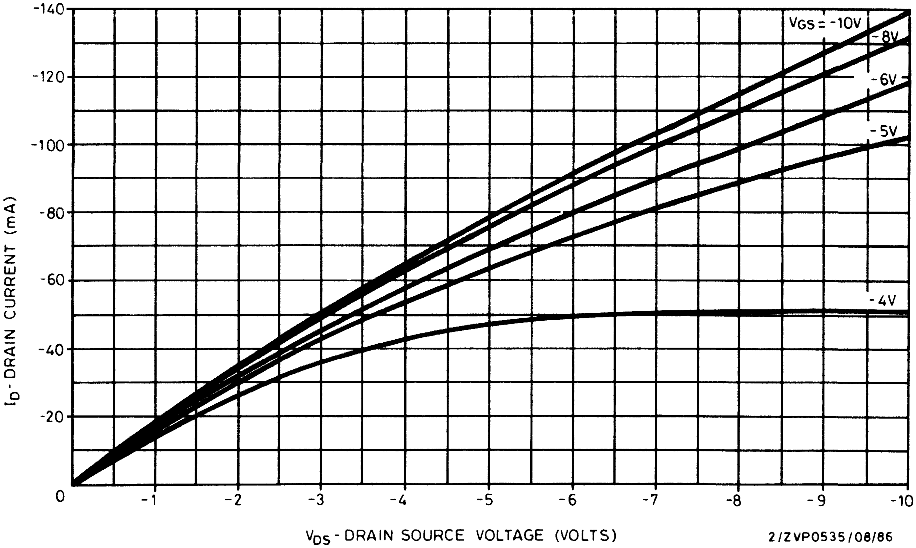


Fig. 2 Typical saturation characteristics

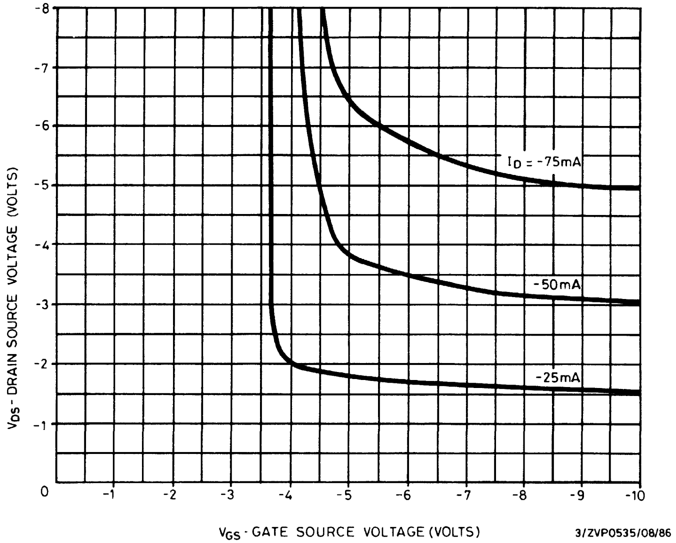


Fig. 3 Typical voltage saturation characteristics

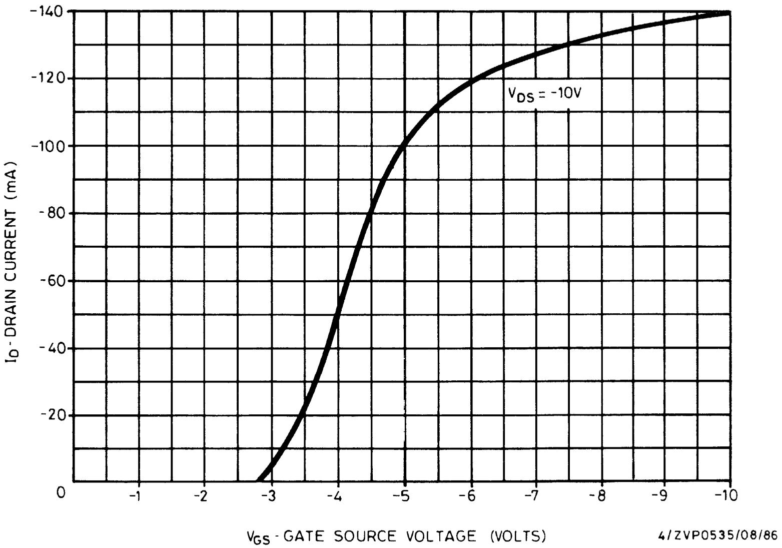


Fig. 4 Typical transfer characteristics

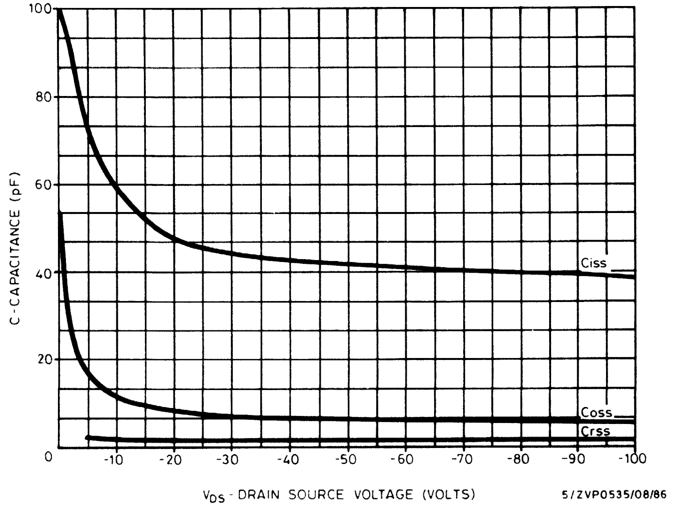


Fig. 5 Typical capacitance v drain-source voltage

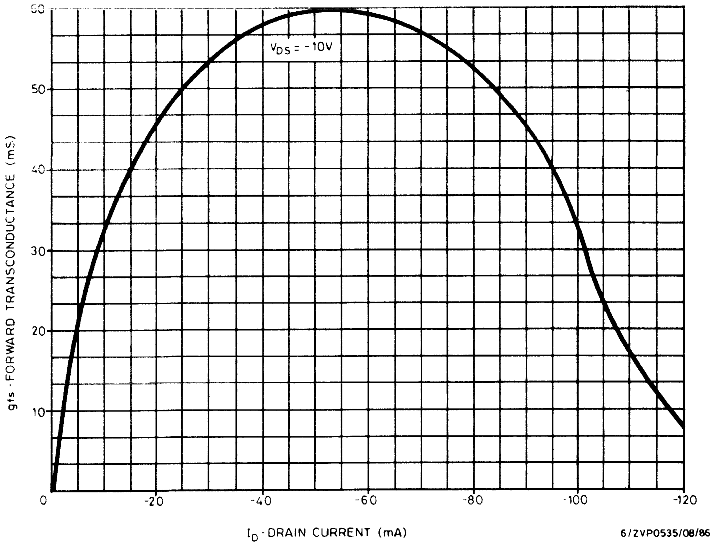


Fig. 6 Typical transconductance v drain current

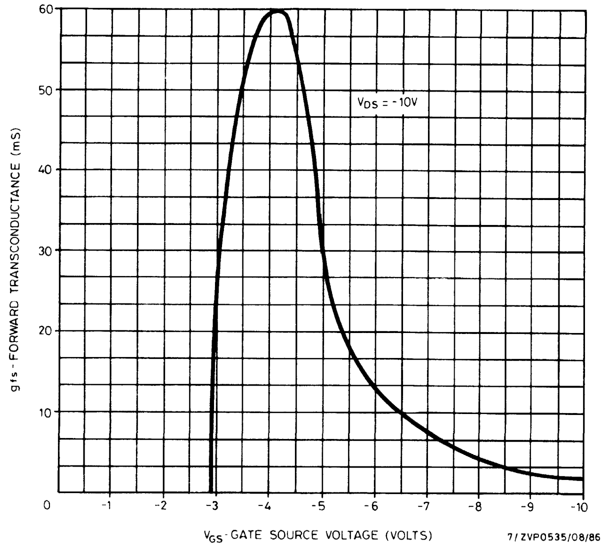


Fig. 7 Typical transconductance v gate-source voltage

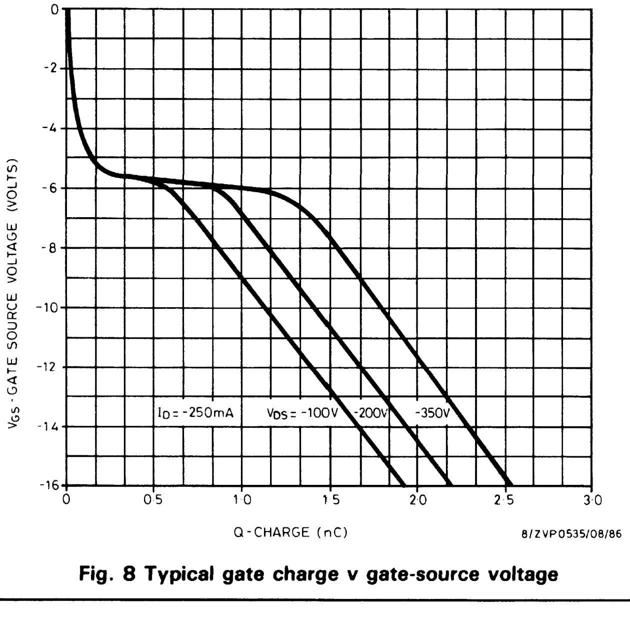


Fig. 8 Typical gate charge v gate-source voltage

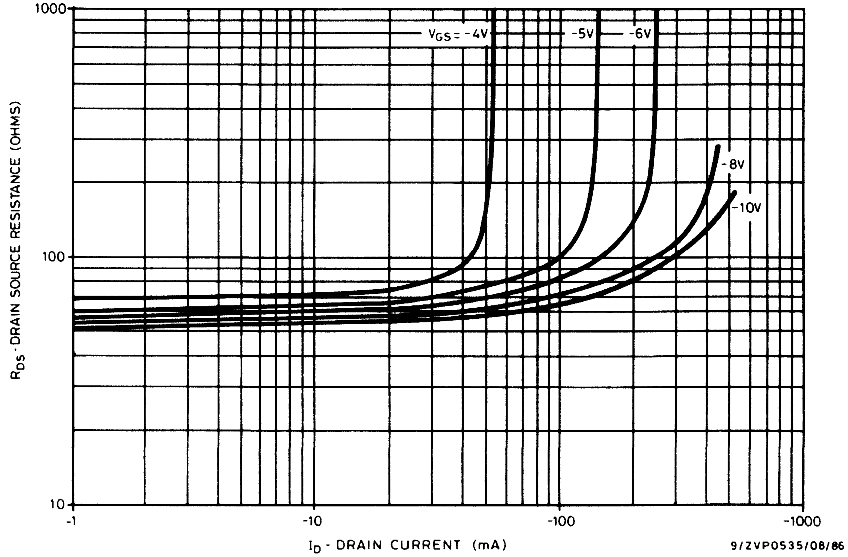


Fig. 9 Typical on-resistance v drain current

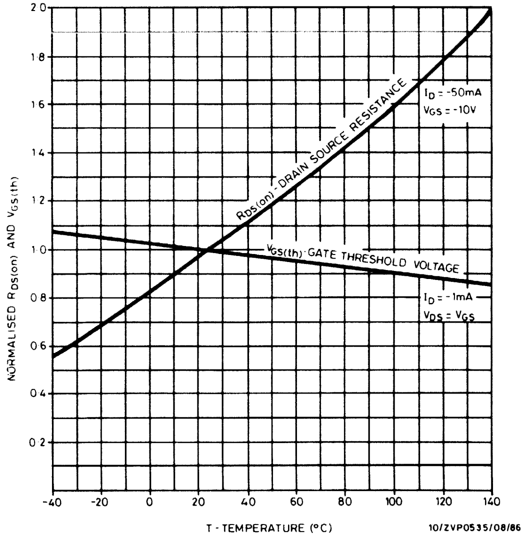


Fig. 10 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

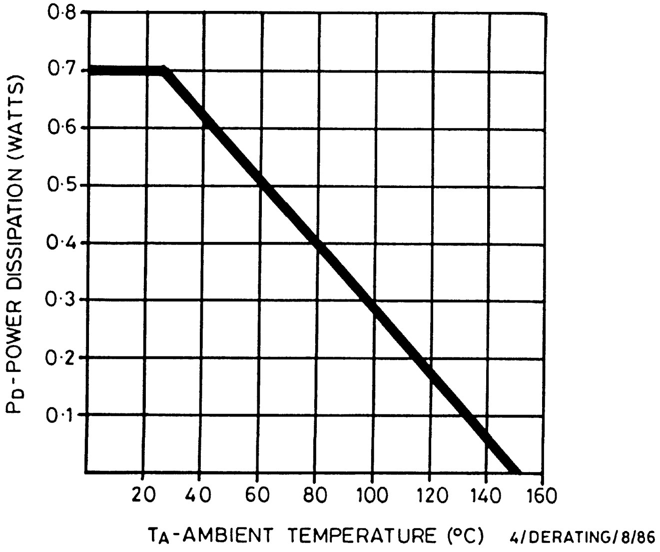


Fig. 11 Power v temperature derating curve (ambient)

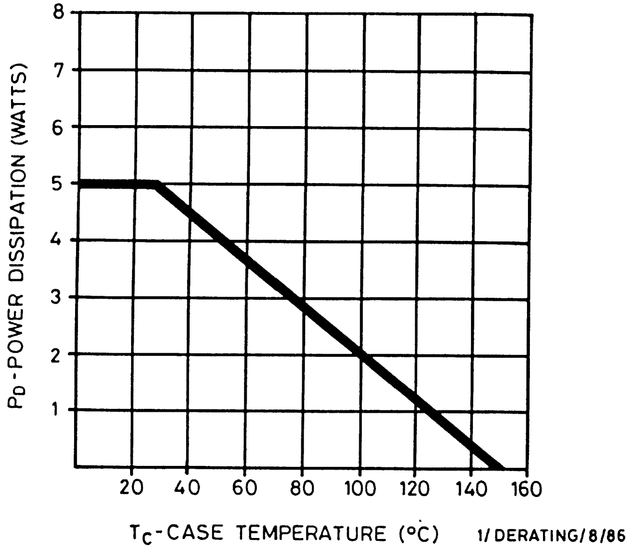


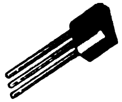
Fig. 12 Power v temperature derating curve (case)

P-channel enhancement mode vertical DMOS FET

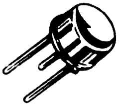
ZVP0540

FEATURES

- **Compact geometry**
- **Fast switching speeds**
- **No secondary breakdown**
- **Excellent temperature stability**
- **High input impedance**
- **Low current drive**
- **Ease of paralleling**



E-LINE (TO-92)
SUFFIX A



TO-39
SUFFIX B

DESCRIPTION

A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVP0540A	−400V	−0.045 A	150Ω
ZVP0540B	−400V	−0.1 A	150Ω

ZVP0540

ABSOLUTE MAXIMUM RATINGS

	Parameters	E-line	TO-39	Unit
V_{DS}	Drain-source voltage	−400	−400	V
I_D	Continuous drain current (@ $T_A = 25°C$)	−0.045	−0.045	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	−0.100	A
I_{DM}	Pulsed drain current	−0.40	−0.40	A
V_{GS}	Gate-source voltage	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	0.7	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

	Parameter	Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	−400	–	V	$I_D = -1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	−1.5	−4.5	V	$I_D = -1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	−20	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	−2	mA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	−100	–	mA	$V_{DS} = -25V$, $V_{GS} = -10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	150	Ω	$I_D = -50mA$, $V_{GS} = -10V$
g_{fs}	Forward transconductance (1) (2)	40	–	mS	$V_{DS} = -25V$, $I_D = -50mA$
C_{iss}	Input capacitance (2)	–	120	pF	$V_{DS} = -25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	20	pF	
C_{rss}	Reverse transfer capacitance (2)	–	5	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	10	ns	$V_{DD} \approx -25V$, $I_D = -50mA$
t_r	Rise time (2) (3)	–	15	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	15	ns	
t_f	Fall time (2) (3)	–	20	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.

(2) Sample test.

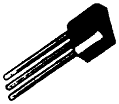
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

P-channel enhancement mode vertical DMOS FET

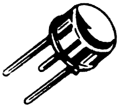
ZVP0545

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)
SUFFIX A



TO-39
SUFFIX B

DESCRIPTION

A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVP0545A	−450V	−0.045 A	150Ω
ZVP0545B	−450V	−0.1 A	150Ω

ZVP0545

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	TO-39	Unit
V_{DS}	Drain-source voltage	−450	−450	V
I_D	Continuous drain current (@ $T_A=25°C$)	−0.045	−0.045	A
I_D	Continuous drain current (@ $T_C=25°C$)	—	−0.100	A
I_{DM}	Pulsed drain current	−0.40	−0.40	A
V_{GS}	Gate-source voltage	±20	±20	V
P_D	Max. power dissipation (@ $T_A=25°C$)	0.7	0.7	W
P_D	Max. power dissipation (@ $T_C=25°C$)	—	5	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	−450	–	V	$I_D = -1mA$, $V_{GS}=0V$
$V_{GS(th)}$	Gate-source threshold voltage	−1.5	−4.5	V	$I_D = -1mA$, $V_{DS}=V_{GS}$
I_{GSS}	Gate body leakage	–	20	nA	$V_{GS}= \pm 20V$, $V_{DS}=0V$
I_{DSS}	Zero gate voltage drain current	–	−20	μA	V_{DS} = Max. rating, $V_{GS}=0V$
		–	−2	mA	V_{DS} = 0.8 × Max. rating $V_{GS}=0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	−100	–	mA	$V_{DS}= -25V$, $V_{GS}= -10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	150	Ω	$I_D= -50mA$, $V_{GS}= -10V$
g_{fs}	Forward transconductance (1) (2)	40	–	mS	$V_{DS}= -25V$, $I_D= -50mA$
C_{iss}	Input capacitance (2)	–	120	pF	$V_{DS}= -25V$, $V_{GS}=0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	20	pF	
C_{rss}	Reverse transfer capacitance (2)	–	5	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	10	ns	$V_{DD} \approx -25V$, $I_D= -50mA$
t_r	Rise time (2) (3)	–	15	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	15	ns	
t_f	Fall time (2) (3)	–	20	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.

(2) Sample test.

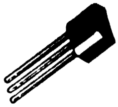
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

P-channel enhancement mode vertical DMOS FET

ZVP1320

FEATURES

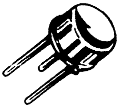
- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



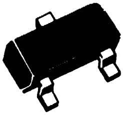
E-LINE (TO-92)
SUFFIX A

DESCRIPTION

A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.



TO-39
SUFFIX B



SOT-23
SUFFIX F

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVP1320A	−200V	−0.07 A	80Ω
ZVP1320B	−200V	−0.10 A	80Ω
ZVP1320F	−200V	−0.035 A	80Ω

ZVP1320

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	TO-39	SOT-23	Units
V_{DS}	Drain-source voltage	−200	−200	−200	V
I_D	Continuous drain current (@ $T_A = 25°C$)	−0.07	−0.07	−0.035	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	−0.10	–	A
I_{DM}	Pulsed drain current	−0.4	−0.4	−0.4	A
V_{GS}	Gate-source voltage	±20	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.625	0.625	0.25	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	–	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150			°C

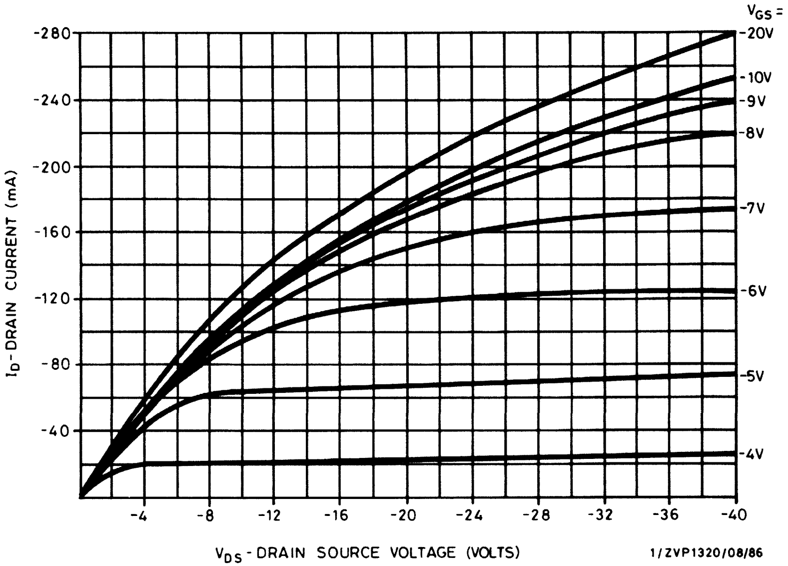
ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	−200	–	V	$I_D = -1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	−1.5	−3.5	V	$I_D = -1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate-body leakage	–	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	−10	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	−50	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	−100	–	mA	$V_{DS} = -25V$, $V_{GS} = -10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	80	Ω	$I_D = -50mA$, $V_{GS} = -10V$
g_{fs}	Forward transconductance (1) (2)	25	–	mS	$V_{DS} = -25V$, $I_D = -50mA$
C_{iss}	Input capacitance (2)	–	50	pF	$V_{DS} = -25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	15	pF	
C_{rss}	Reverse transfer capacitance (2)	–	5	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	8	ns	$V_{DD} \approx -25V$, $I_D = -50mA$
t_r	Rise time (2) (3)	–	8	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	8	ns	
t_f	Fall time (2) (3)	–	16	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ≤ 2%.

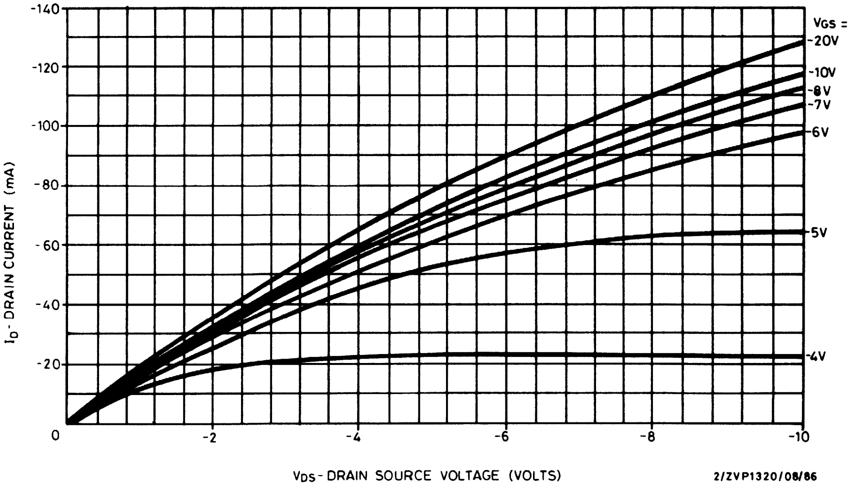
(2) Sample test.

(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.



1/ZVP1320/08/86

Fig. 1 Typical output characteristics



2/ZVP1320/08/86

Fig. 2 Typical saturation characteristics

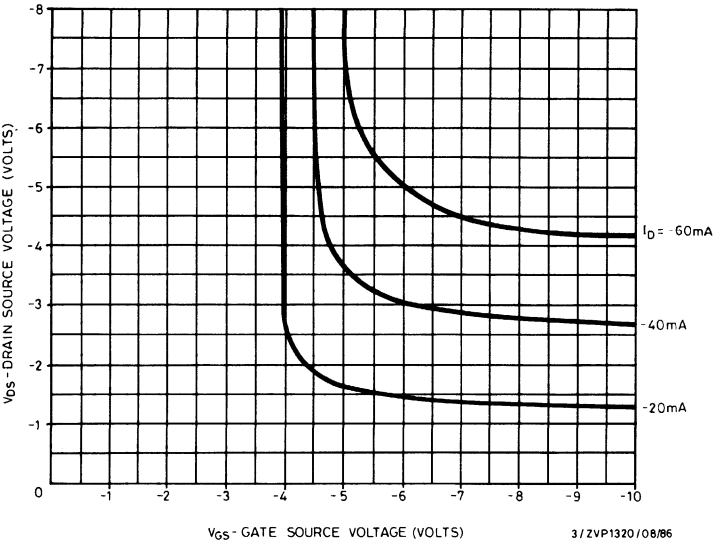


Fig. 3 Typical voltage saturation characteristics

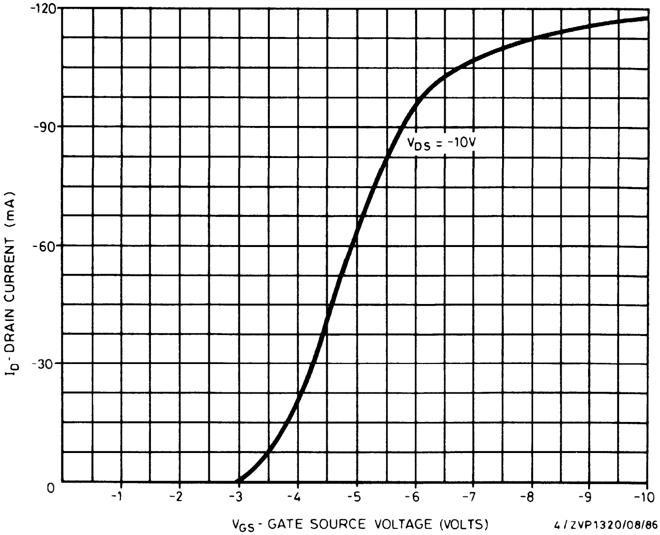


Fig. 4 Typical transfer characteristics

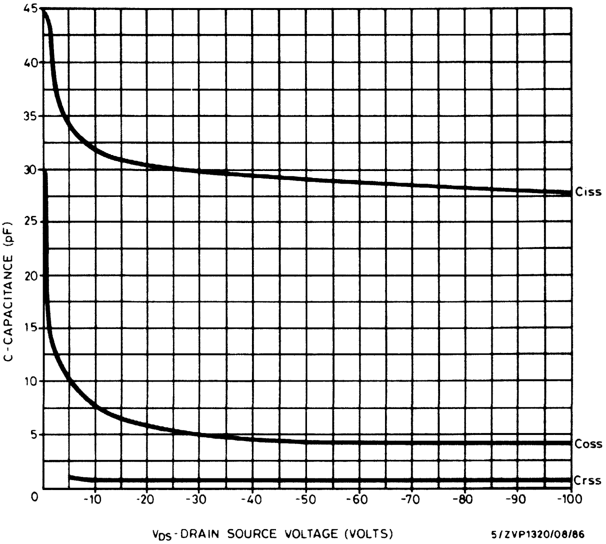


Fig. 5 Typical capacitance v drain-source voltage

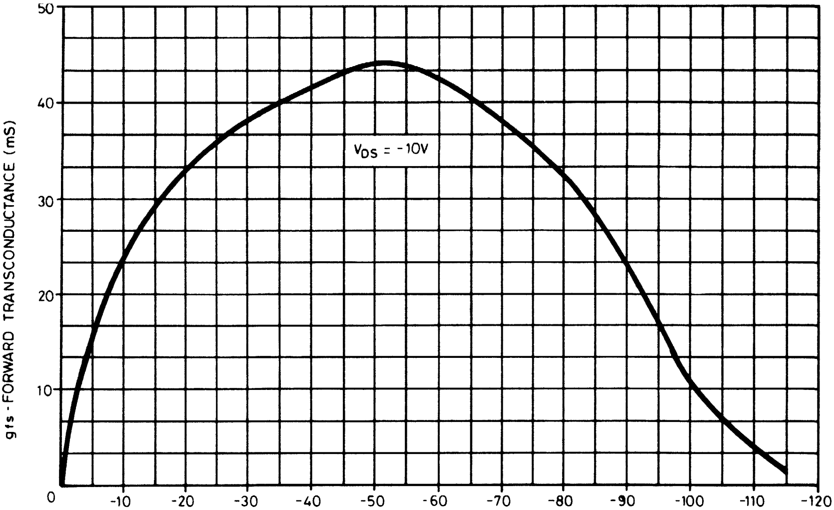


Fig. 6 Typical transconductance v drain current

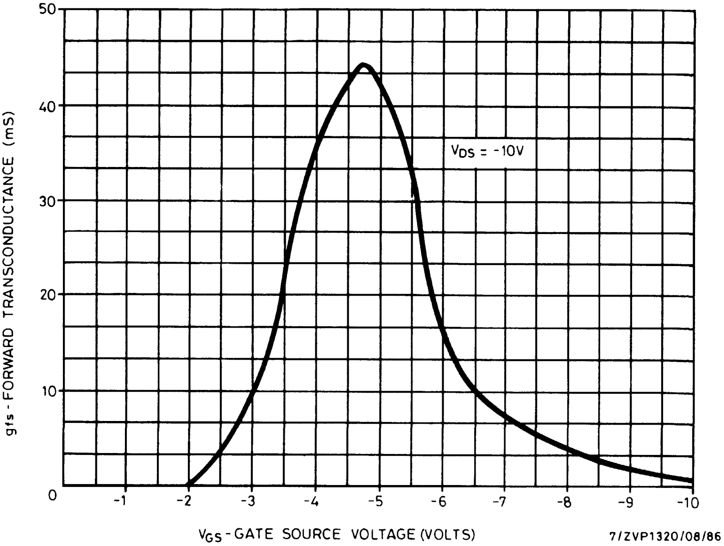


Fig. 7 Typical transconductance v gate-source voltage

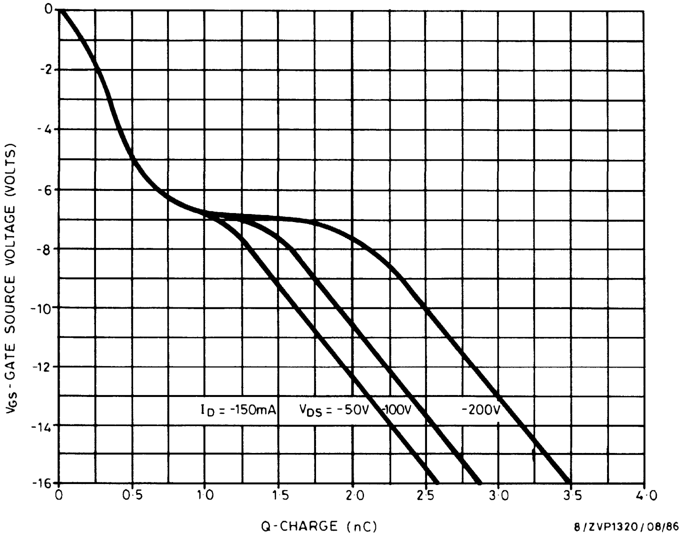


Fig. 8 Typical gate charge v gate-source voltage

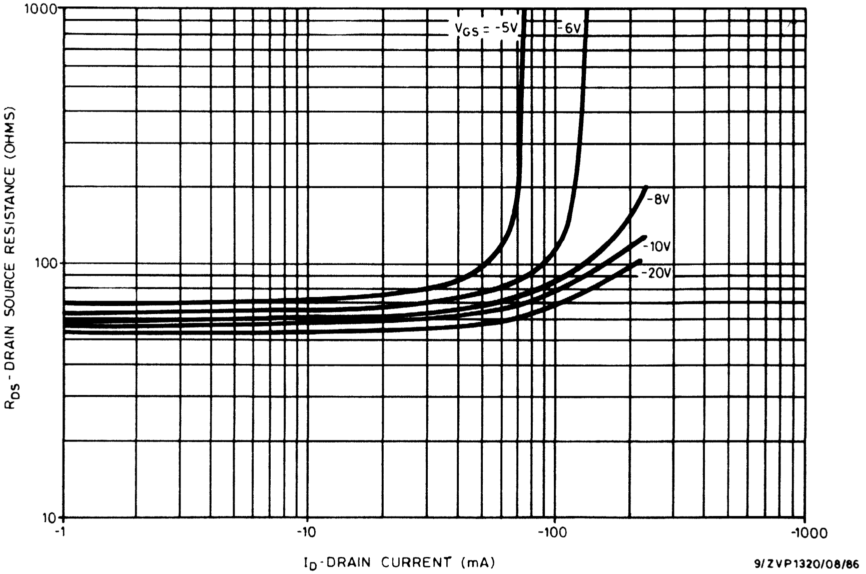


Fig. 9 Typical on-resistance v drain current

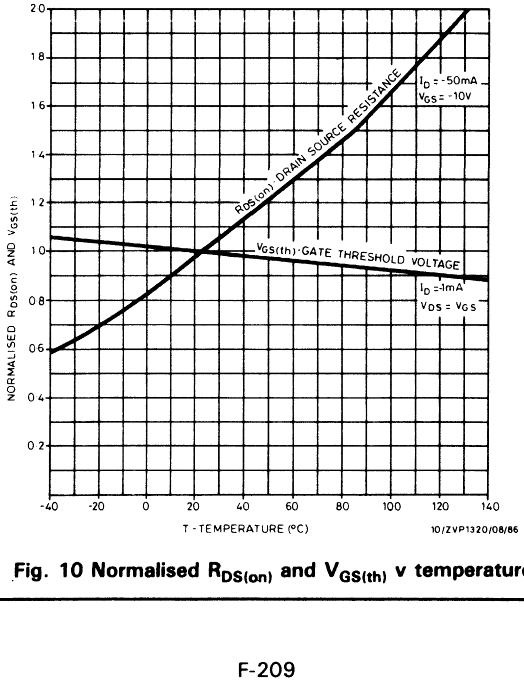


Fig. 10 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

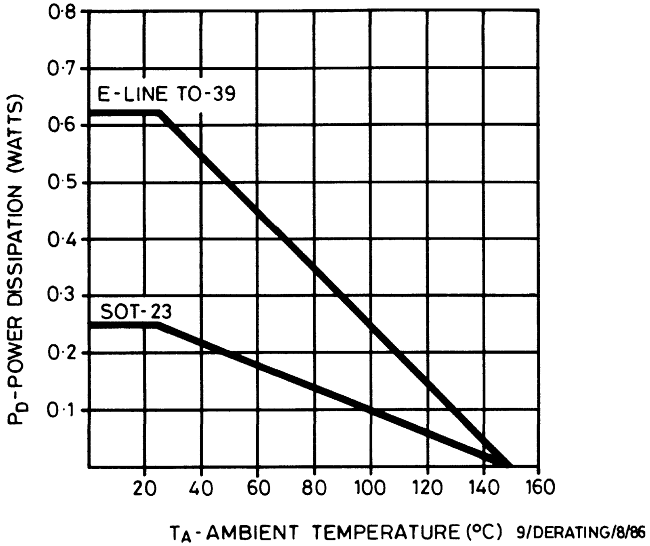


Fig. 11 Power v temperature derating curve (ambient)

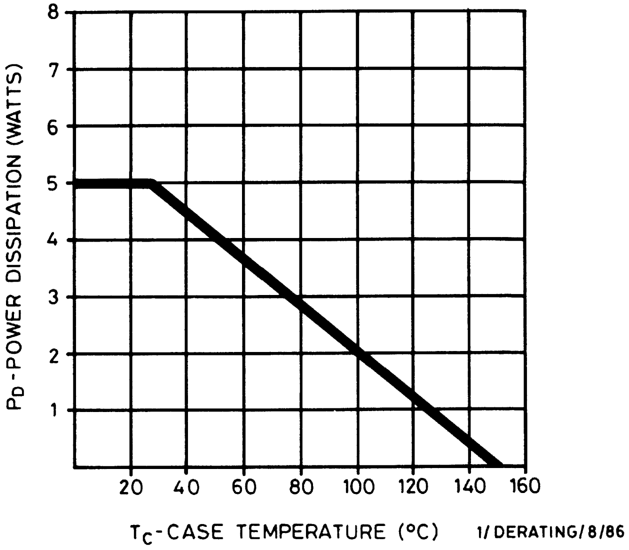


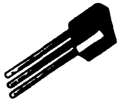
Fig. 12 Power v temperature derating curve (case)

P-Channel enhancement mode vertical DMOS FET

ZVP2106

FEATURES

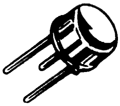
- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



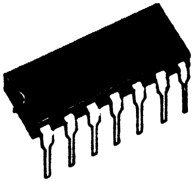
E-LINE (TO-92)
SUFFIX A or C

DESCRIPTION

A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.



TO-39
SUFFIX B

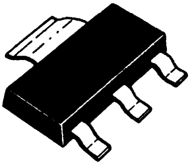


14 LEAD MOULDED DIL
SUFFIX E

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVP2106A*	−60V	−0.28A	5Ω
ZVP2106B*	−60V	−0.76A	5Ω
ZVP2106C	−60V	−0.28A	5Ω
ZVP2106E	−60V	−0.28A	5Ω
ZVP2106G	−60V	−0.45A	5Ω

*BS-CECC approved



SOT-223
SUFFIX G

ZVP2106

ABSOLUTE MAXIMUM RATINGS

	Parameters	E-line	TO-39	DIL	SOT-223	Units
V_{DS}	Drain-source voltage	−60	−60	−60	−60	V
I_D	Continuous drain current (@ $T_A = 25°C$)	−0.28	−0.28	−0.28	−0.45	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	−0.76	–	–	A
I_{DM}	Pulsed drain current	−4	−4	−3	−4	A
V_{GS}	Gate-source voltage	±20	±20	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	0.7	0.85	2	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	–	–	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150				°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

	Parameter	Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	−60	–	V	$I_D = -1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	−1.5	−3.5	V	$I_D = -1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	−0.5	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	−100	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	−1	–	A	$V_{DS} = -18V$, $V_{GS} = -10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	5	Ω	$I_D = -500mA$, $V_{GS} = -10V$
g_{fs}	Forward transconductance (1) (2)	150	–	mS	$V_{DS} = -18V$, $I_D = -500mA$
C_{iss}	Input capacitance (2)	–	100	pF	$V_{DS} = -18V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	60	pF	
C_{rss}	Reverse transfer capacitance (2)	–	20	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	7	ns	$V_{DD} \approx -18V$, $I_D = -500mA$
t_r	Rise time (2) (3)	–	15	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	12	ns	
t_f	Fall time (2) (3)	–	15	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ≤2%.

(2) Sample test.

(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

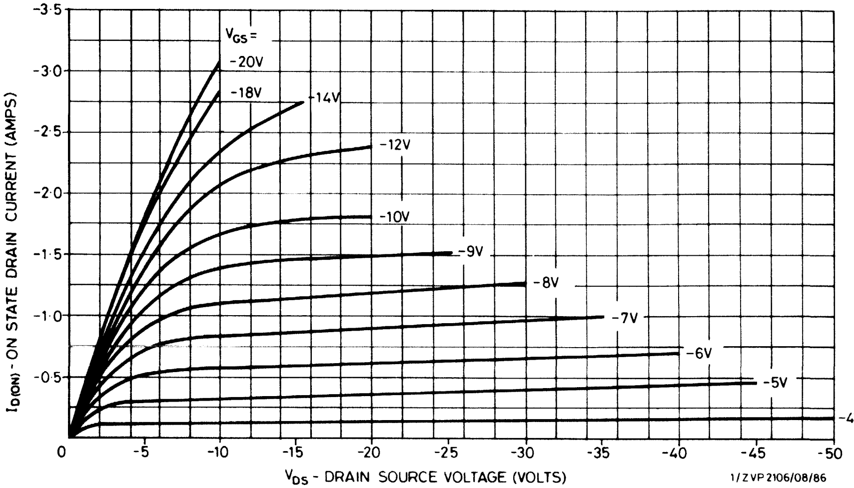


Fig. 1 Typical output characteristics

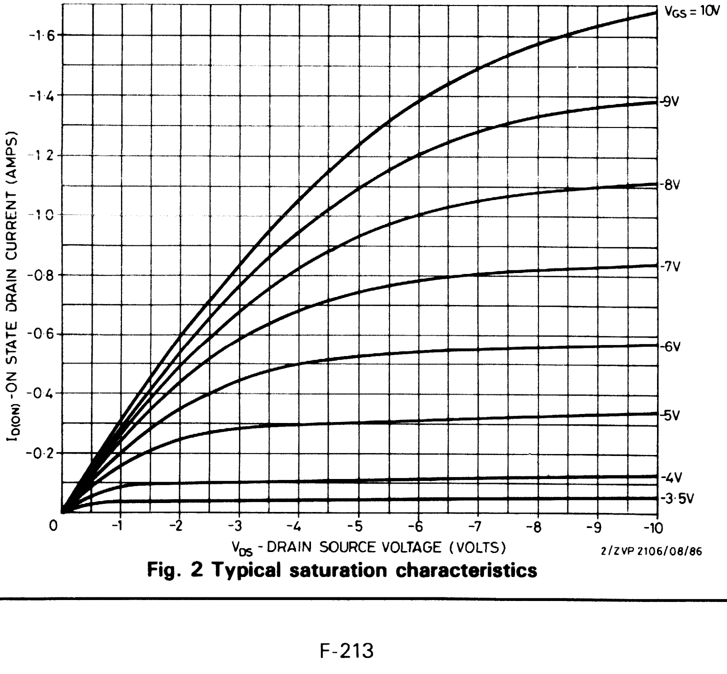


Fig. 2 Typical saturation characteristics

Fig. 3 Typical voltage saturation characteristics

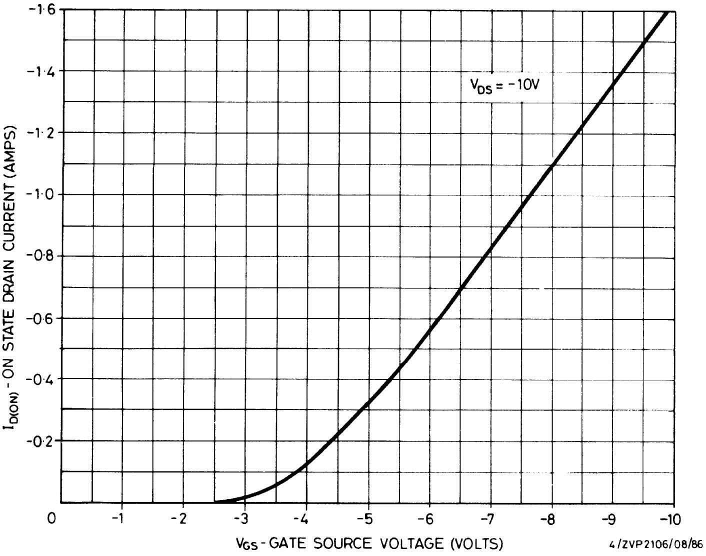


Fig. 4 Typical transfer characteristics

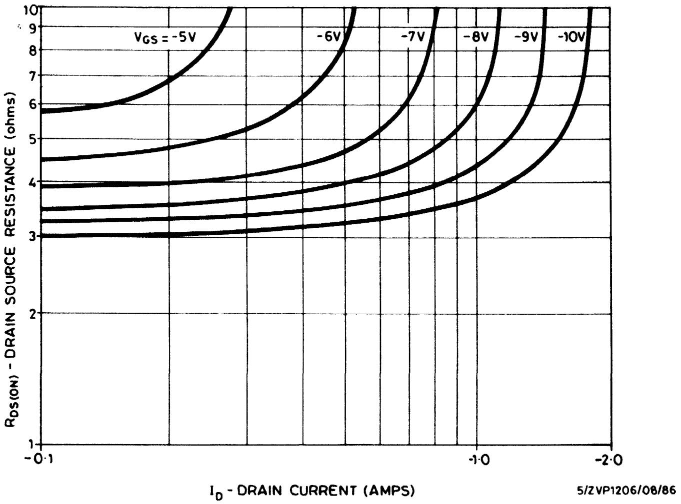


Fig. 5 Typical on-resistance v drain current

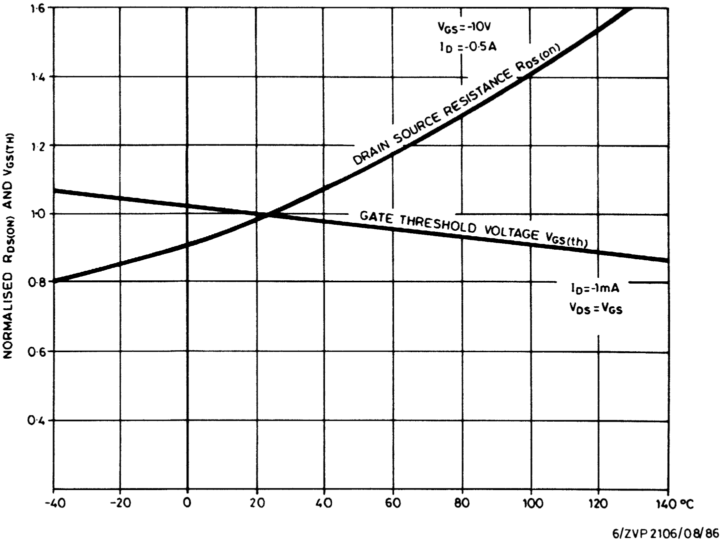


Fig. 6 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

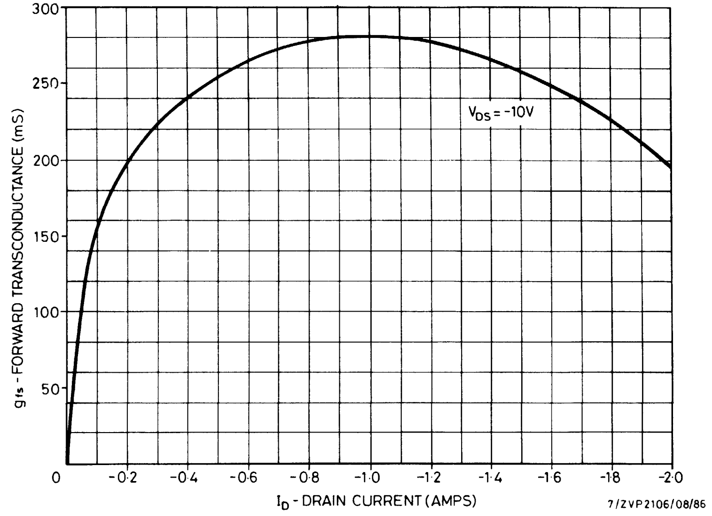


Fig. 7 Typical transconductance v drain current

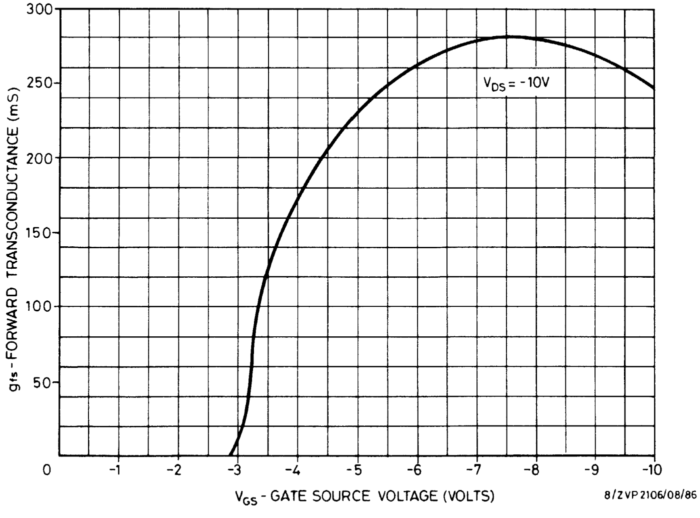


Fig. 8 Typical transconductance v gate-source voltage

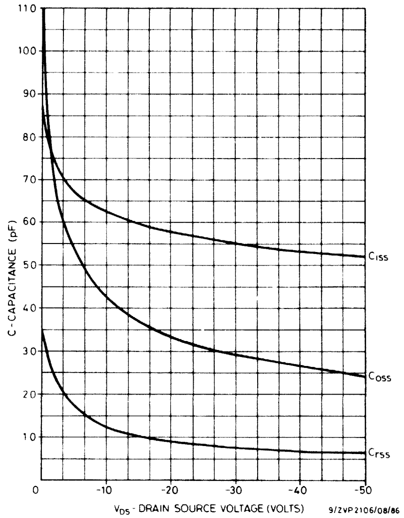


Fig. 9 Typical capacitance v drain-source voltage

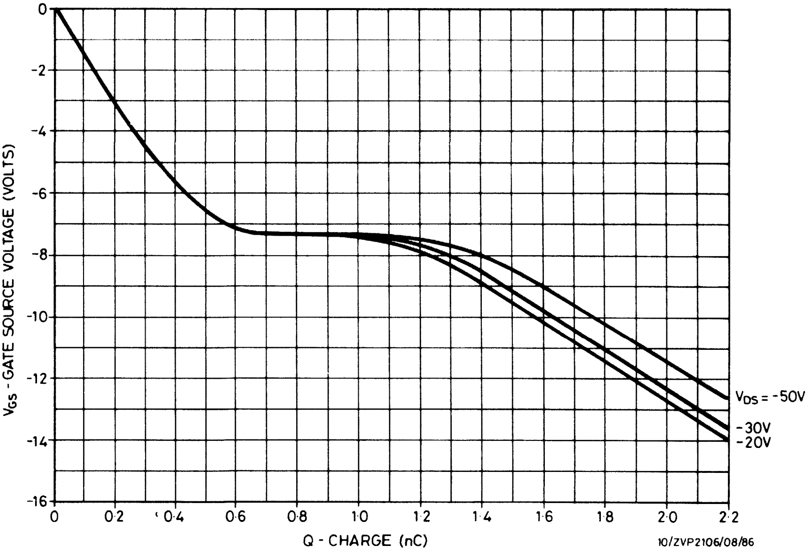


Fig. 10 Typical gate charge v gate-source voltage

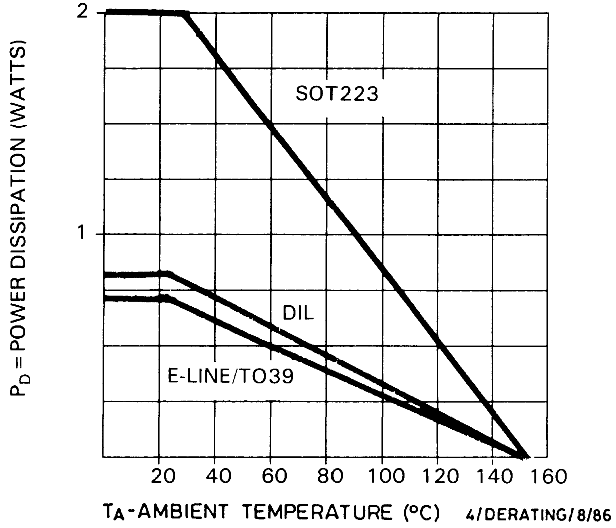


Fig. 11 Power v temperature derating curve (ambient)

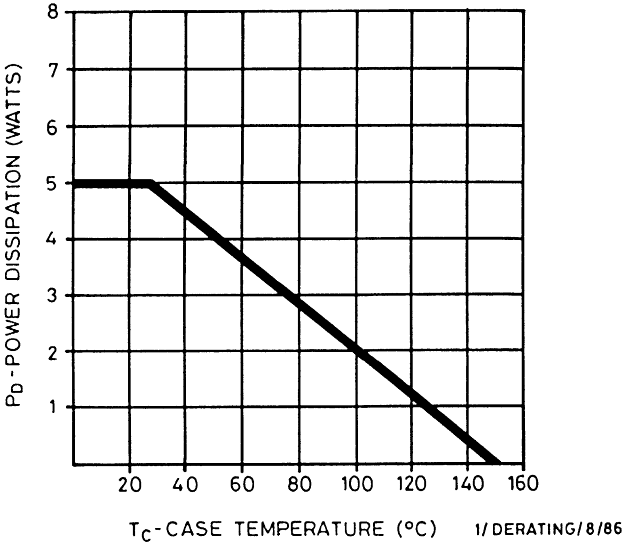


Fig. 12 Power v temperature derating curve (case)

P-channel enhancement mode vertical DMOS FET

ZVP2110

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling

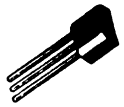
DESCRIPTION

A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

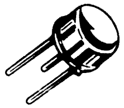
PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVP2110A*	−100V	−0.23A	8Ω
ZVP2110B*	−100V	−0.60A	8Ω
ZVP2110C	−100V	−0.23A	8Ω
ZVP2110E	−100V	−0.23A	8Ω

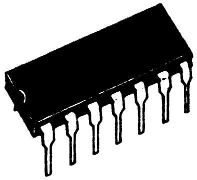
*BS-CECC approved



E-LINE (TO-92)
SUFFIX A or C



TO-39
SUFFIX B



14 LEAD MOULDED DIL
SUFFIX E

ZVP2110

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	TO-39	DIL	Units
V_{DS}	Drain-source voltage	−100	−100	−100	V
I_D	Continuous drain current (@ $T_A = 25°C$)	−0.23	−0.23	−0.23	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	−0.60	–	A
I_{DM}	Pulsed drain current	−3	−3	−3	A
V_{GS}	Gate-source voltage	±20	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	0.7	0.85	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	–	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150			°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	−100	–	V	$I_D = -1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	−1.5	−3.5	V	$I_D = -1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	−1	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	−100	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	−750	–	mA	$V_{DS} = -25V$, $V_{GS} = -10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	8	Ω	$I_D = -375mA$, $V_{GS} = -10V$
g_{fs}	Forward transconductance (1) (2)	125	–	mS	$V_{DS} = -25V$, $I_D = -375mA$
C_{iss}	Input capacitance (2)	–	100	pF	$V_{DS} = -25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	35	pF	
C_{rss}	Reverse transfer capacitance (2)	–	10	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	7	ns	$V_{DD} \approx -25V$, $I_D = -375mA$
t_r	Rise time (2) (3)	–	15	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	12	ns	
t_f	Fall time (2) (3)	–	15	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.

(2) Sample test.

(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

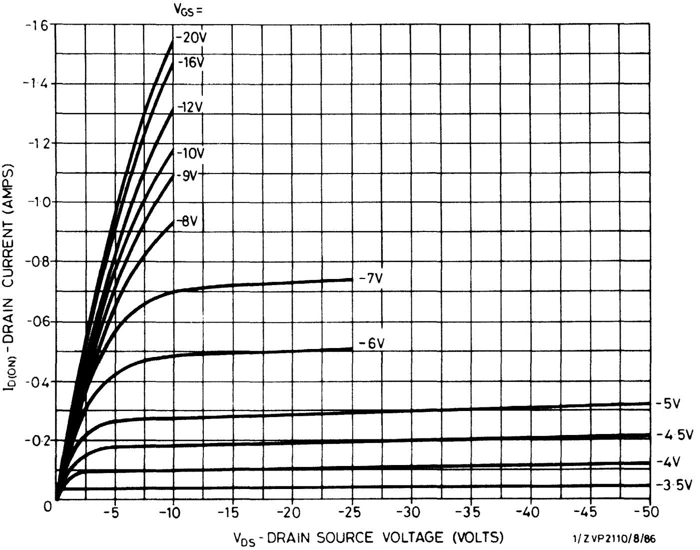


Fig. 1 Typical output characteristics

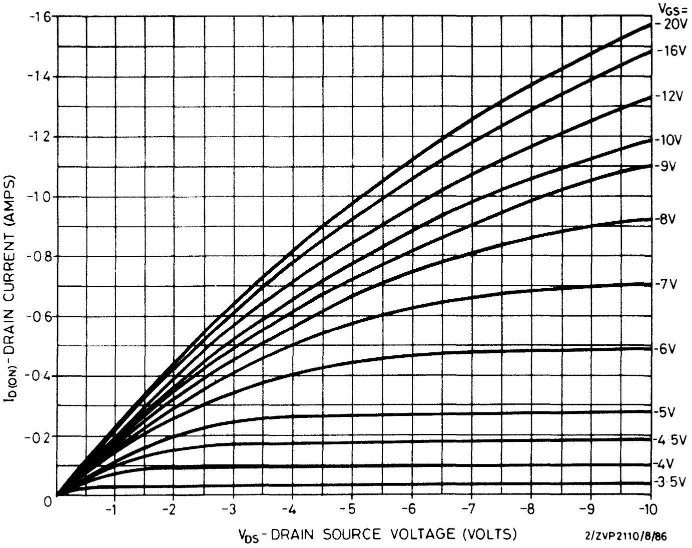


Fig. 2 Typical saturation characteristics

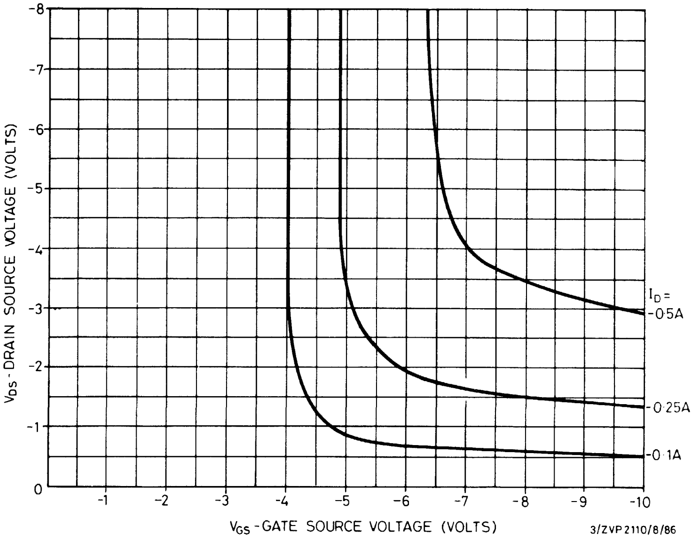


Fig. 3 Typical voltage saturation characteristics

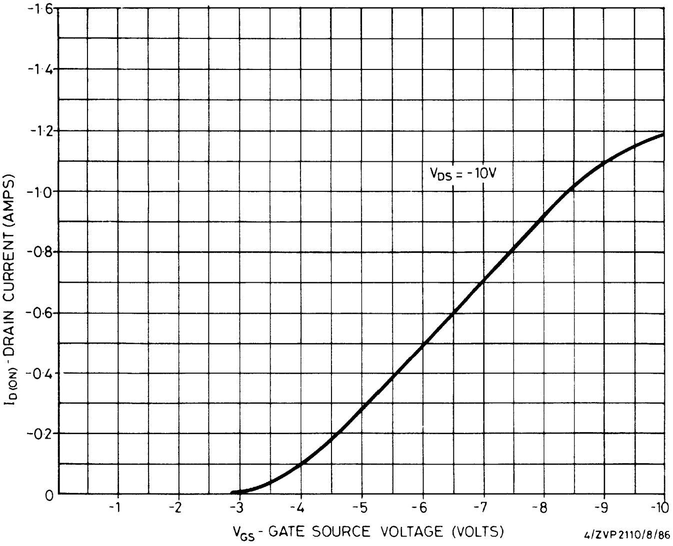


Fig. 4 Typical transfer characteristics

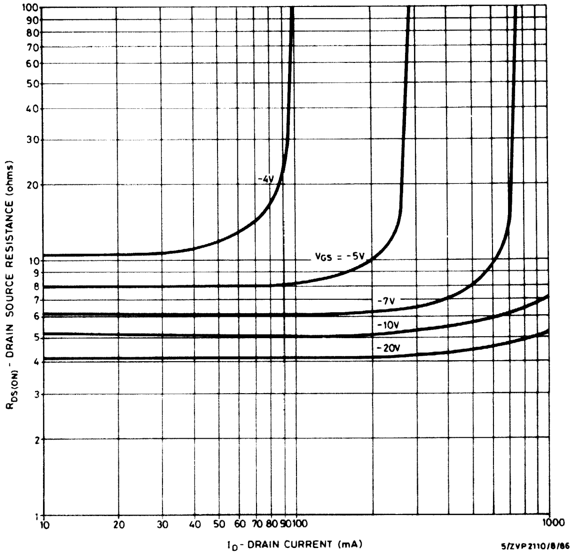


Fig. 5 Typical on-resistance v drain current

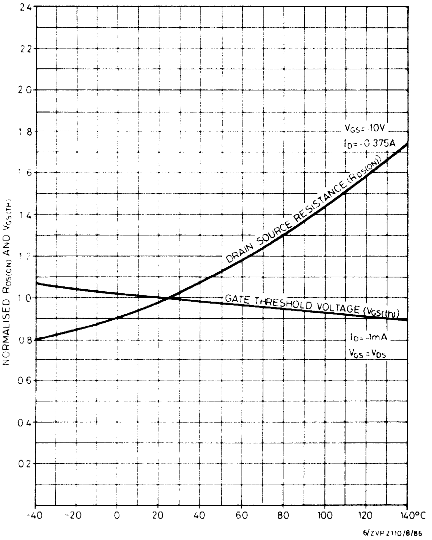


Fig. 6 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

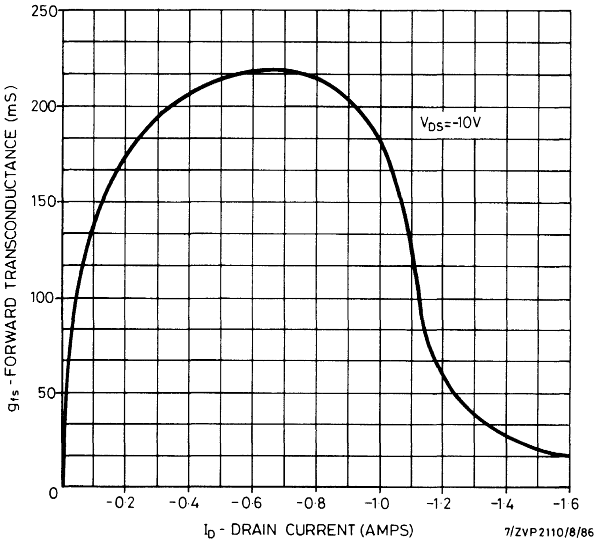


Fig. 7 Typical transconductance v drain current

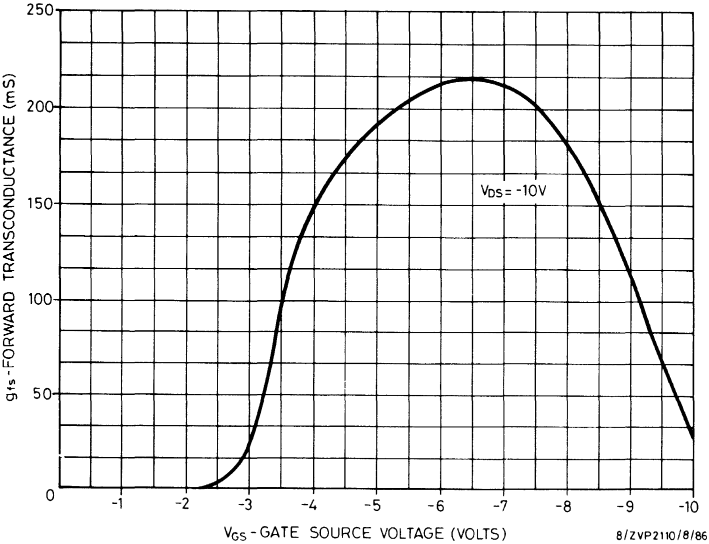


Fig. 8 Typical transconductance v gate-source voltage

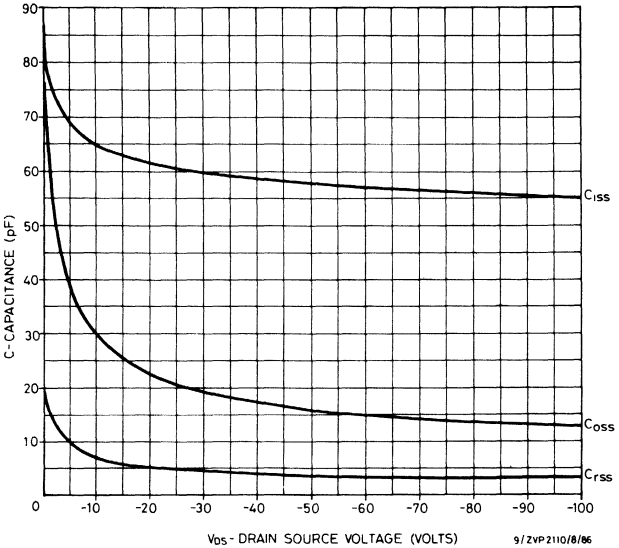


Fig. 9 Typical capacitance v drain-source voltage

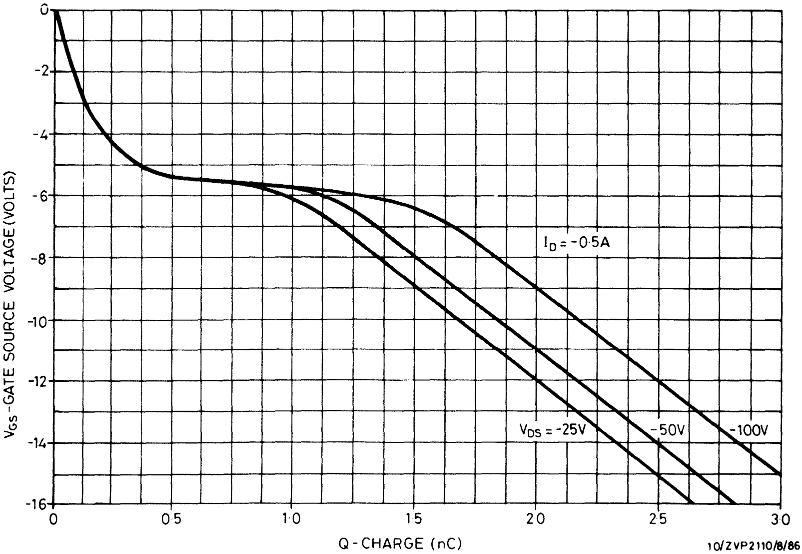


Fig. 10 Typical gate charge v gate-source voltage

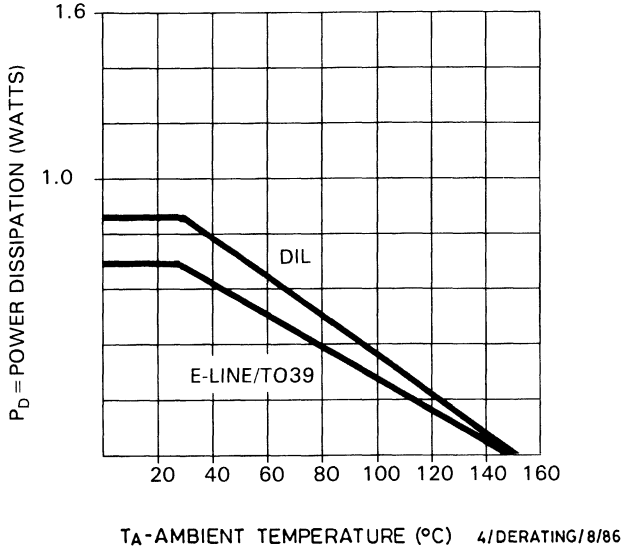


Fig. 11 Power v temperature derating curve (ambient)

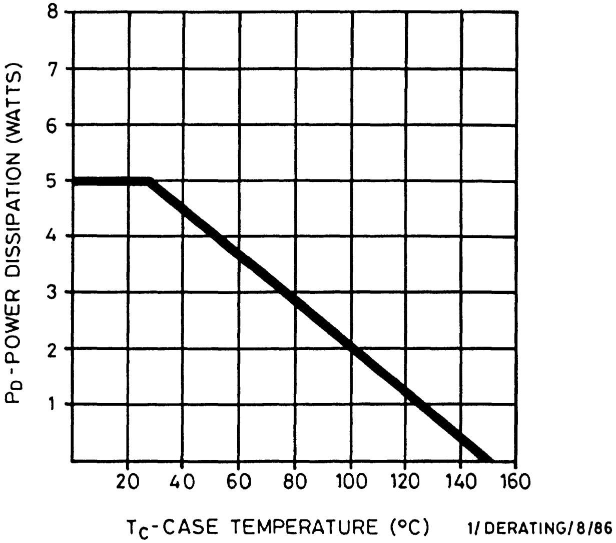


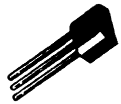
Fig. 12 Power v temperature derating curve (case)

P-channel enhancement mode vertical DMOS FET

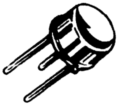
ZVP2120

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)
SUFFIX A or C



TO-39
SUFFIX B

DESCRIPTION

A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVP2120A	−200V	−0.12A	25Ω
ZVP2120B	−200V	−0.3A	25Ω
ZVP2120C	−200V	−0.12A	25Ω

ZVP2120

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	TO-39	Unit
V_{DS}	Drain-source voltage	−200	−200	V
I_D	Continuous drain current (@ $T_A = 25°C$)	−0.12	−0.12	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	−0.3	A
I_{DM}	Pulsed drain current	−1.2	−1.2	A
V_{GS}	Gate-source voltage	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	0.7	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	−200	–	V	$I_D = -1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	−1.5	−3.5	V	$I_D = -1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	−10	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	−100	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	−300	–	mA	$V_{DS} = -25V$, $V_{GS} = -10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	25	Ω	$I_D = -150mA$, $V_{GS} = -10V$
g_{fs}	Forward transconductance (1) (2)	50	–	mS	$V_{DS} = -25V$, $I_D = -150mA$
C_{iss}	Input capacitance (2)	–	100	pF	$V_{DS} = -25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	25	pF	
C_{rss}	Reverse transfer capacitance (2)	–	7	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	7	ns	$V_{DD} \approx -25V$, $I_D = -150mA$
t_r	Rise time (2) (3)	–	15	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	12	ns	
t_f	Fall time (2) (3)	–	15	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.

(2) Sample test.

(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

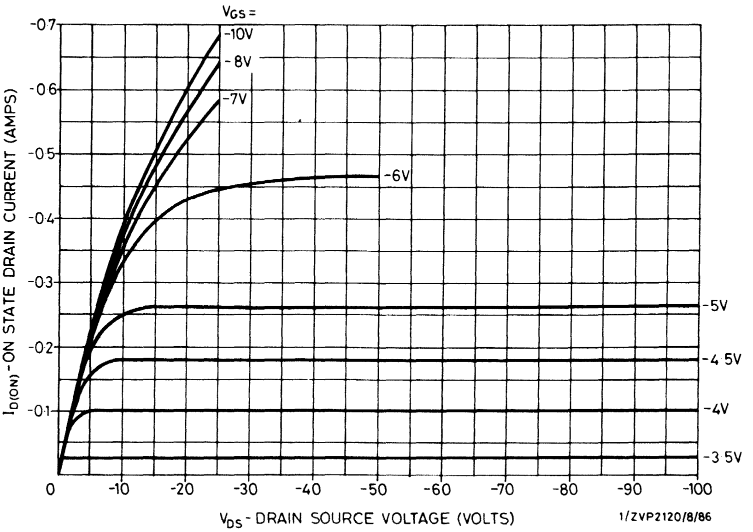


Fig. 1 Typical output characteristics

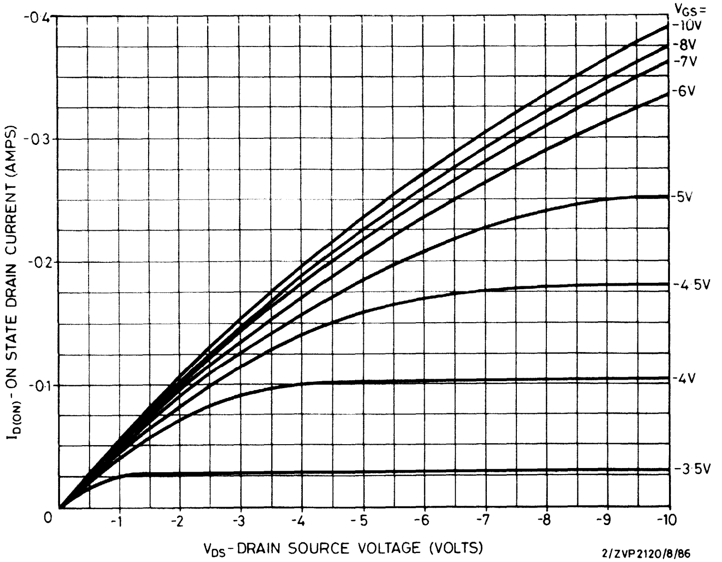


Fig. 2 Typical saturation characteristics

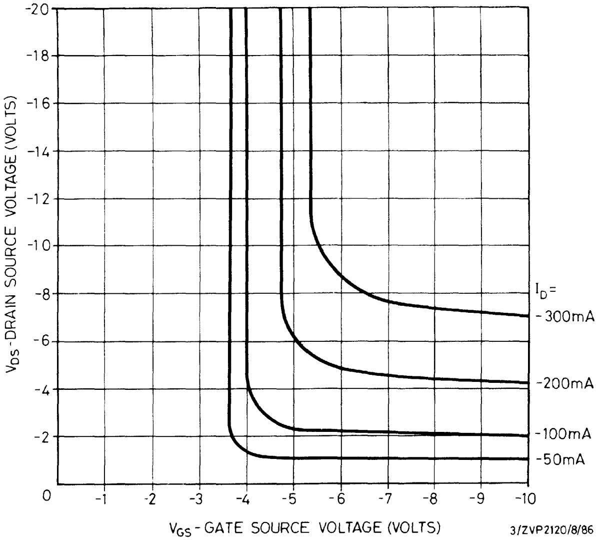


Fig. 3 Typical voltage saturation characteristics

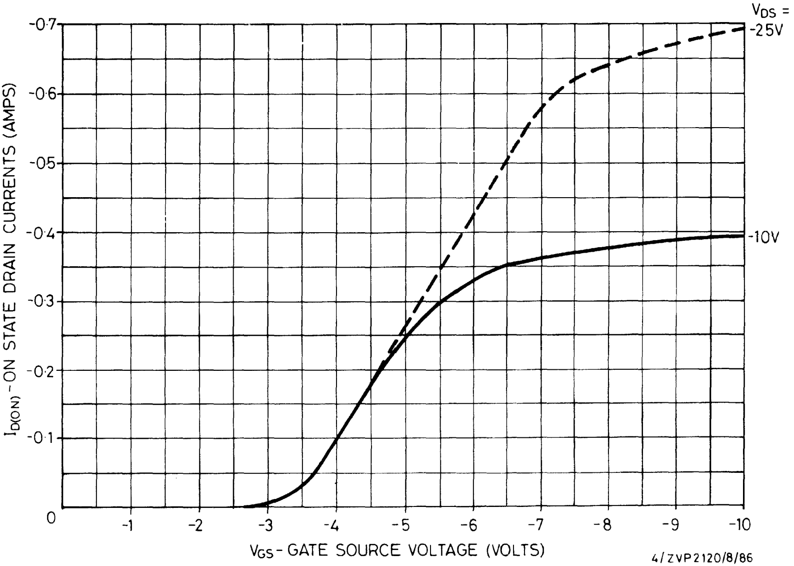


Fig. 4 Typical transfer characteristics

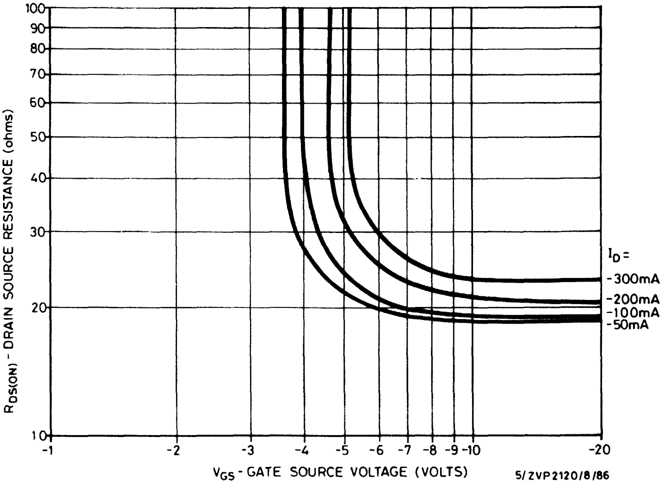


Fig. 5 Typical on-resistance v gate-source voltage

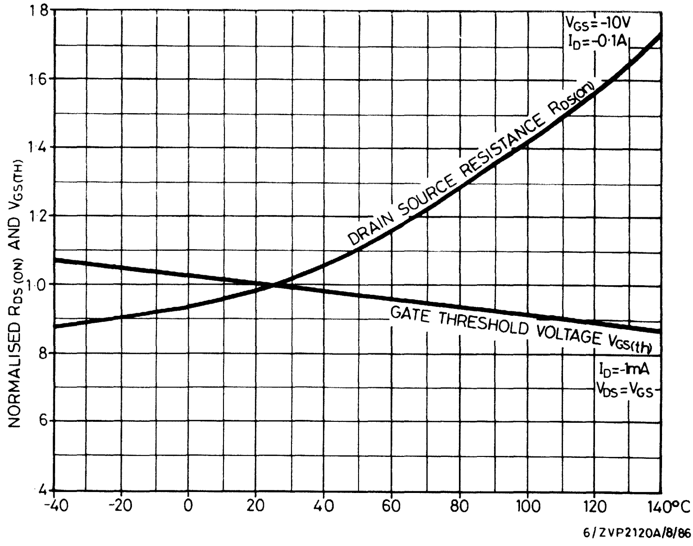


Fig. 6 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

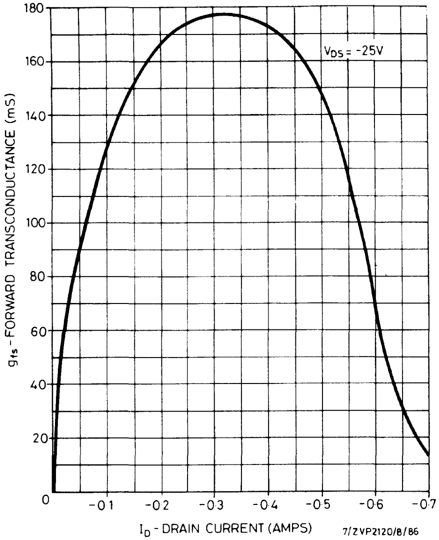


Fig. 7 Typical transconductance v drain current

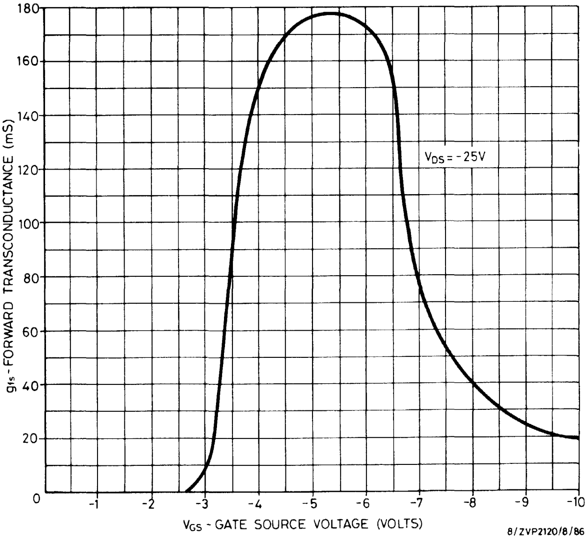


Fig. 8 Typical transconductance v gate-source voltage

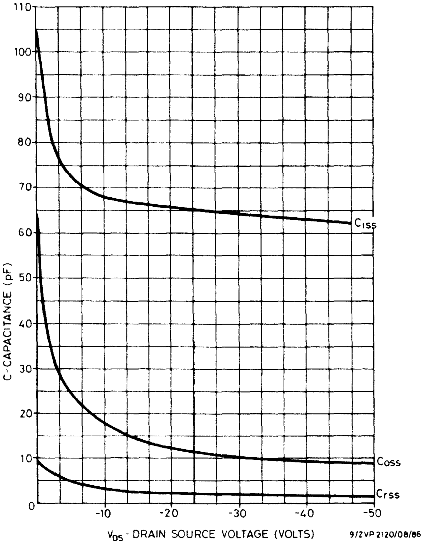


Fig. 9 Typical capacitance v drain-source voltage

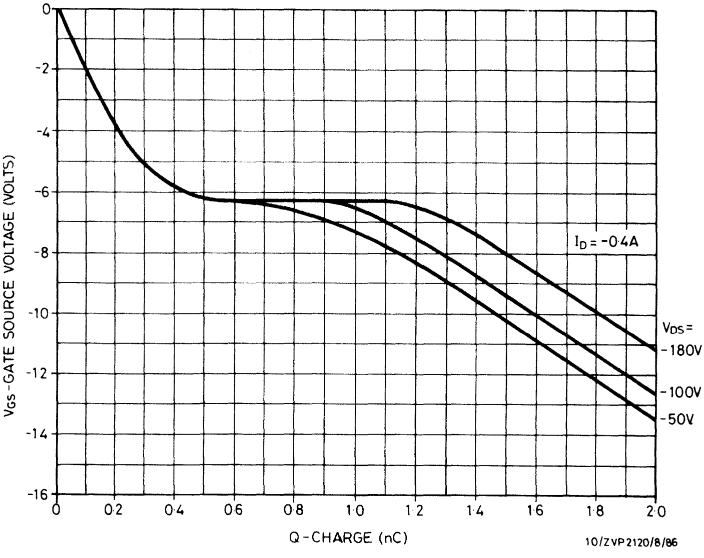


Fig. 10 Typical gate charge v gate-source voltage

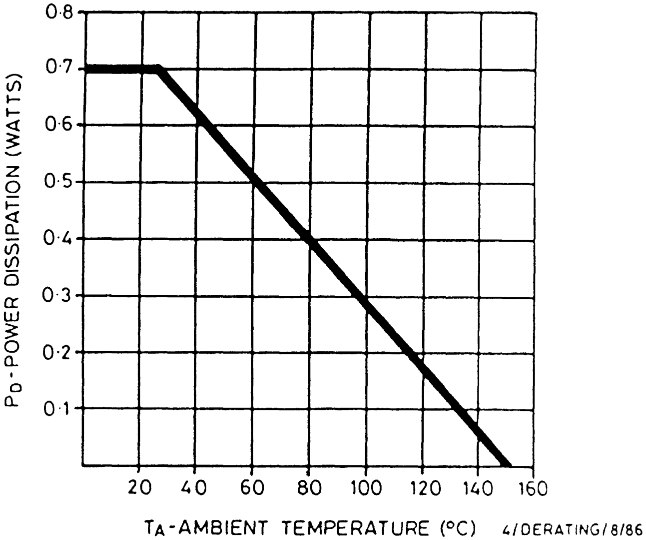


Fig. 11 Power v temperature derating curve (ambient)

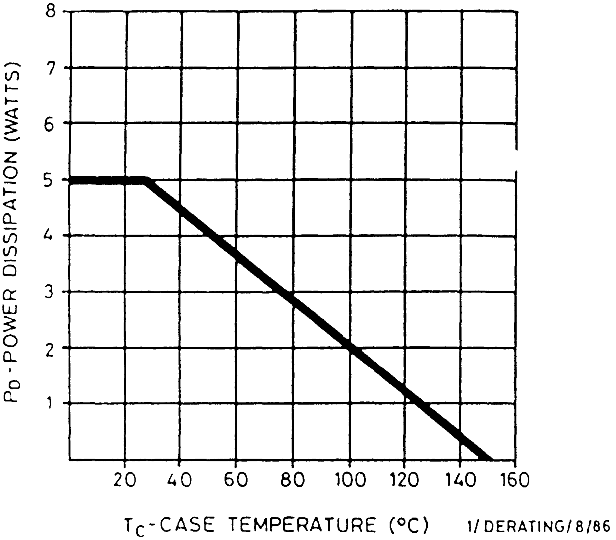
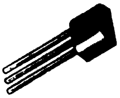


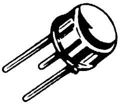
Fig. 12 Power v temperature derating curve (case)

P-channel enhancement mode vertical DMOS FET

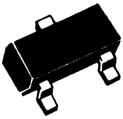
ZVP3306



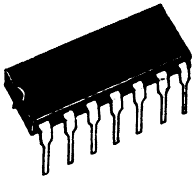
E-LINE (TO-92)
SUFFIX A



TO-39
SUFFIX B



SOT-23
SUFFIX F



14 LEAD MOULDED DIL
SUFFIX E

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling

DESCRIPTION

A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVP3306A	−60V	−0.16A	14Ω
ZVP3306B	−60V	−0.4A	14Ω
ZVP3306F	−60V	−0.09A	14Ω
ZVP3306E	−60V	−0.16A	14Ω

ZVP3306

ABSOLUTE MAXIMUM RATINGS

	Parameters	E-line	TO-39	SOT-23	DIL	Units
V_{DS}	Drain-source voltage	−60	−60	−60	−60	V
I_D	Continuous drain current (@ $T_A=25°C$)	−0.16	−0.16	−0.09	−0.16	A
I_D	Continuous drain current (@ $T_C=25°C$)	–	−0.4	–	–	A
I_{DM}	Pulsed drain current	−1.6	−1.6	−1.6	−1.6	A
V_{GS}	Gate-source voltage	±20	±20	±20	±20	V
P_D	Max. power dissipation (@ $T_A=25°C$)	0.625	0.625	0.25	0.85	W
P_D	Max. power dissipation (@ $T_C=25°C$)	–	5	–	–	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150				°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

	Parameter	Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	−60	–	V	$I_D = -1mA$, $V_{GS}=0V$
$V_{GS(th)}$	Gate-source threshold voltage	−1.5	−3.5	V	$I_D = -1mA$, $V_{DS}=V_{GS}$
I_{GSS}	Gate body leakage	–	20	nA	$V_{GS}= \pm 20V$, $V_{DS}=0V$
I_{DSS}	Zero gate voltage drain current	–	−0.5	μA	V_{DS} = Max. rating, $V_{GS}=0V$
		–	−50	μA	V_{DS} = 0.8 × Max. rating $V_{GS}=0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	−400	–	mA	$V_{DS}= -18V$, $V_{GS}= -10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	14	Ω	$I_D = -200mA$, $V_{GS}= -10V$
g_{fs}	Forward transconductance (1) (2)	60	–	mS	$V_{DS}= -18V$, $I_D= -200mA$
C_{iss}	Input capacitance (2)	–	50	pF	$V_{DS}= -18V$, $V_{GS}=0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	25	pF	
C_{rss}	Reverse transfer capacitance (2)	–	8	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	8	ns	$V_{DD} \approx -18V$, $I_D = -200mA$
t_r	Rise time (2) (3)	–	8	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	8	ns	
t_f	Fall time (2) (3)	–	8	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.

(2) Sample test.

(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

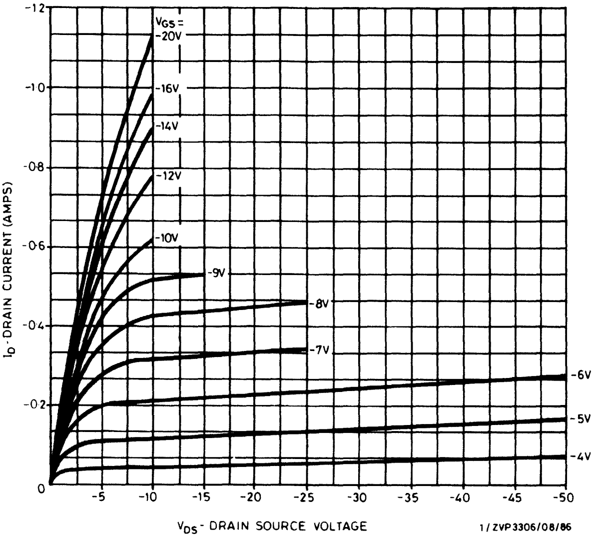


Fig. 1 Typical output characteristics

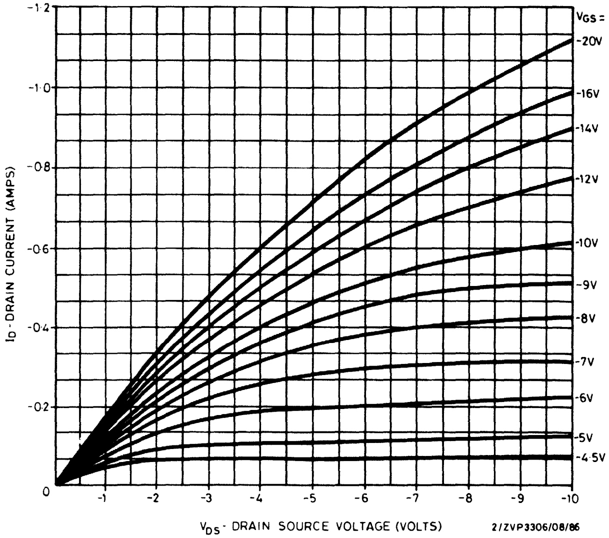


Fig. 2 Typical saturation characteristics

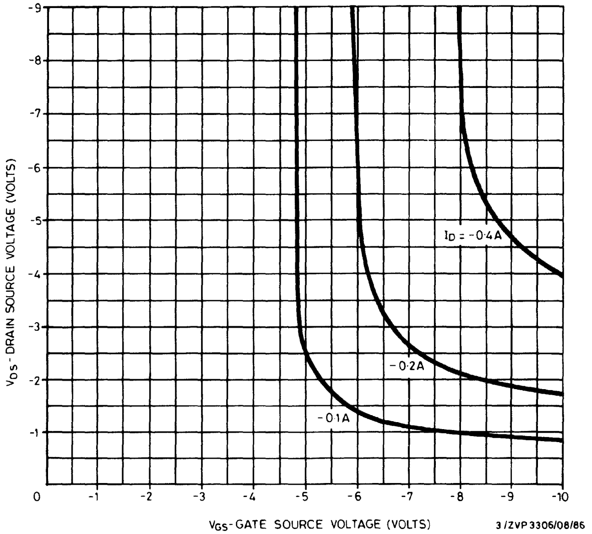


Fig. 3 Typical voltage saturation characteristics

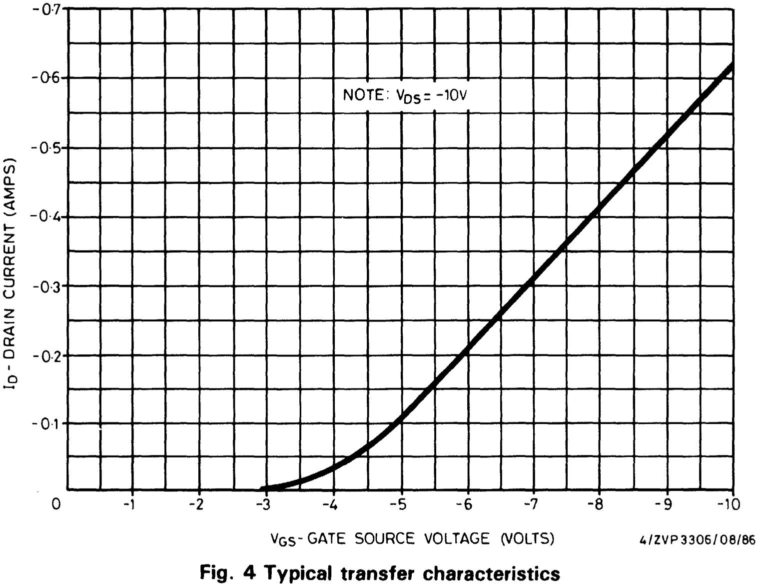
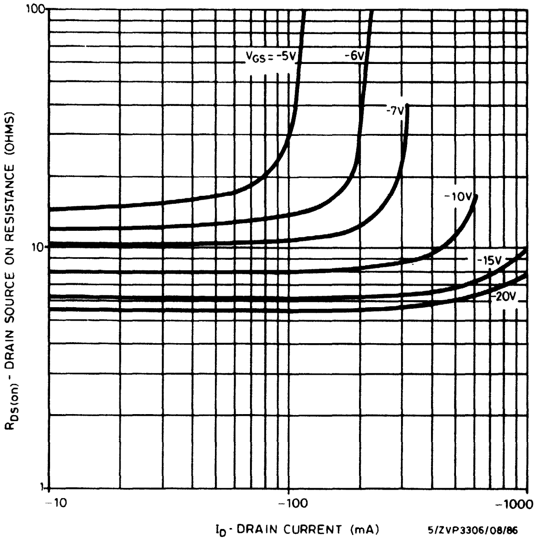
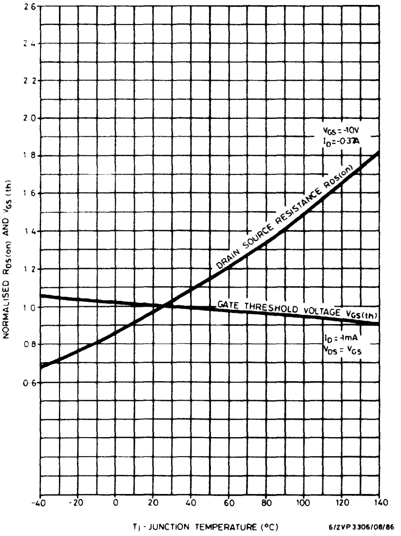


Fig. 4 Typical transfer characteristics



5/ZVP3306/08/86

Fig. 5 Typical on-resistance v drain current



6/ZVP3306/08/86

Fig. 6 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

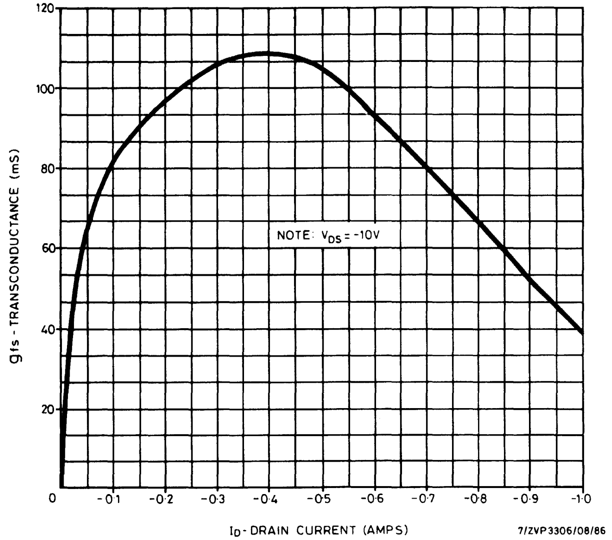


Fig. 7 Typical transconductance v drain current

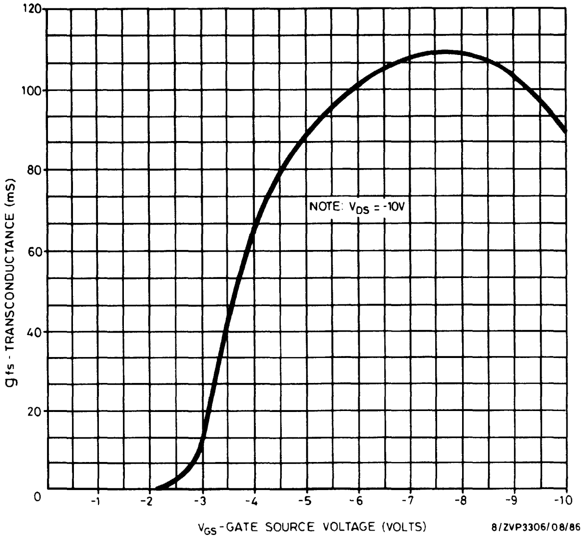


Fig. 8 Typical transconductance v gate-source voltage

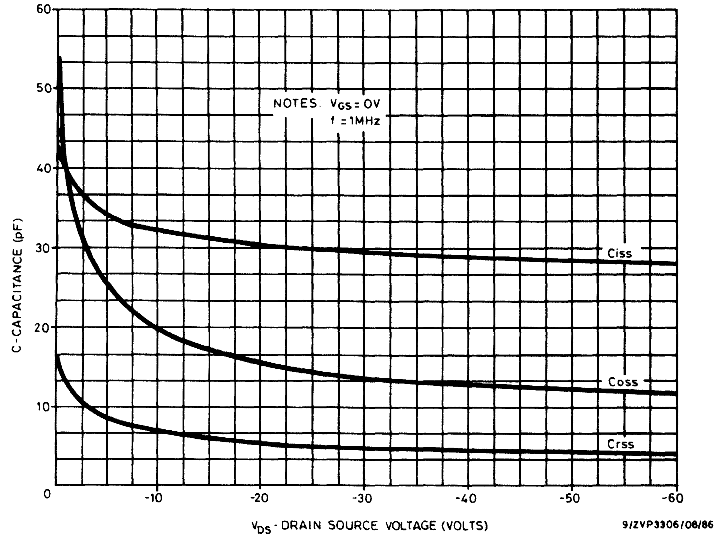


Fig. 9 Typical capacitance v drain-source voltage

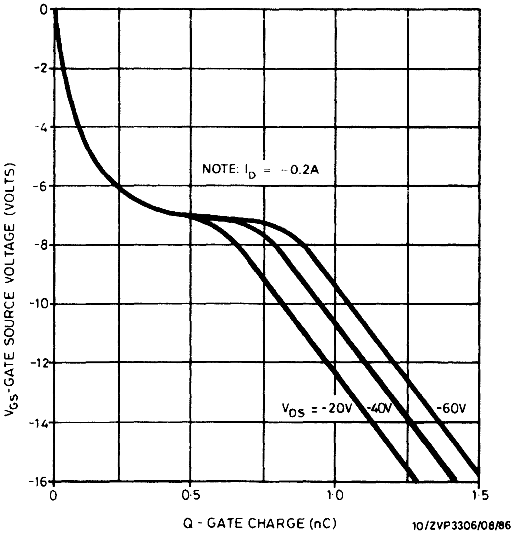


Fig. 10 Typical gate charge v gate-source voltage

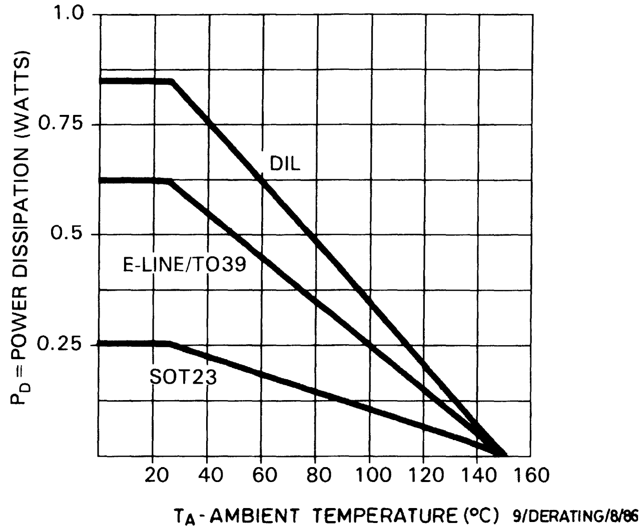


Fig. 11 Power v temperature derating curve (ambient)

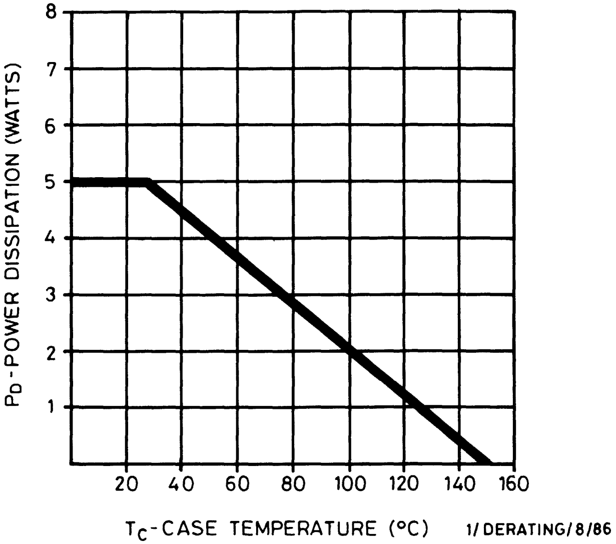


Fig. 12 Power v temperature derating curve (case)

P-channel enhancement mode vertical DMOS FET

ZVP3310

FEATURES

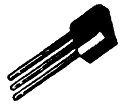
- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling

DESCRIPTION

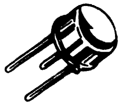
A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

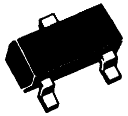
Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVP3310A	−100V	−0.14A	20Ω
ZVP3310B	−100V	−0.3A	20Ω
ZVP3310F	−100V	−0.075A	20Ω



E-LINE (TO-92)
SUFFIX A



TO-39
SUFFIX B



SOT-23
SUFFIX F

ZVP3310

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	TO-39	SOT-23	Units
V_{DS}	Drain-source voltage	−100	−100	−100	V
I_D	Continuous drain current (@ $T_A = 25°C$)	−0.14	−0.14	−0.075	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	−0.3	–	A
I_{DM}	Pulsed drain current	−1.2	−1.2	−1.2	A
V_{GS}	Gate-source voltage	±20	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.625	0.625	0.25	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	–	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150			°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	−100	–	V	$I_D = -1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	−1.5	−3.5	V	$I_D = -1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	−1	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	−50	μA	V_{DS} = 0.8 × Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	−300	–	mA	$V_{DS} = -25V$, $V_{GS} = -10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	20	Ω	$I_D = -150mA$, $V_{GS} = -10V$
g_{fs}	Forward transconductance (1) (2)	50	–	mS	$V_{DS} = -25V$, $I_D = -150mA$
C_{iss}	Input capacitance (2)	–	50	pF	$V_{DS} = -25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	15	pF	
C_{rss}	Reverse transfer capacitance (2)	–	5	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	8	ns	$V_{DD} \approx -25V$, $I_D = -150mA$
t_r	Rise time (2) (3)	–	8	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	8	ns	
t_f	Fall time (2) (3)	–	8	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽2%.

(2) Sample test.

(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

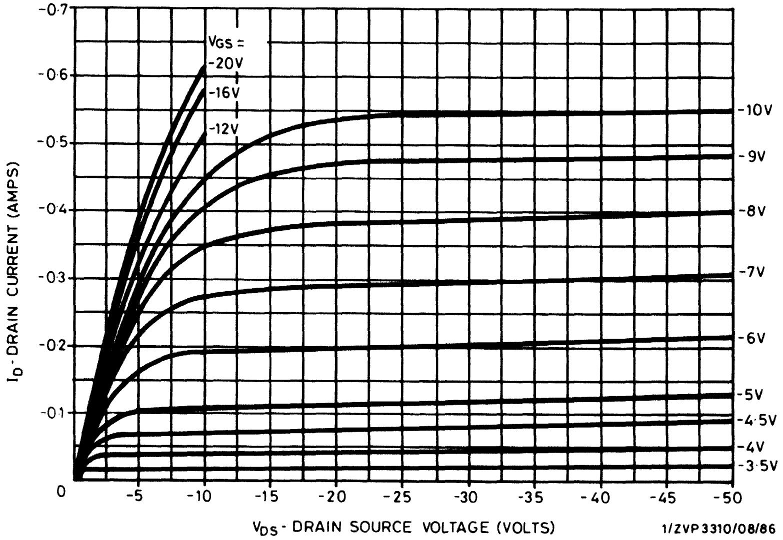


Fig. 1 Typical output characteristics

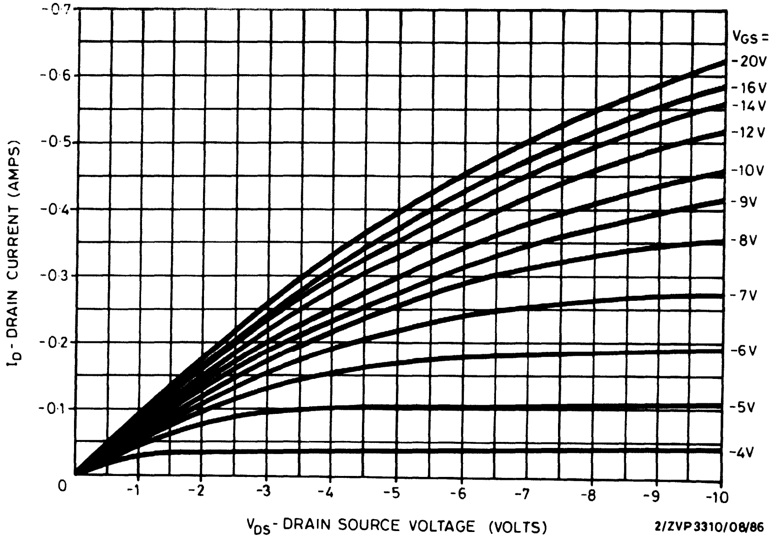


Fig. 2 Typical saturation characteristics

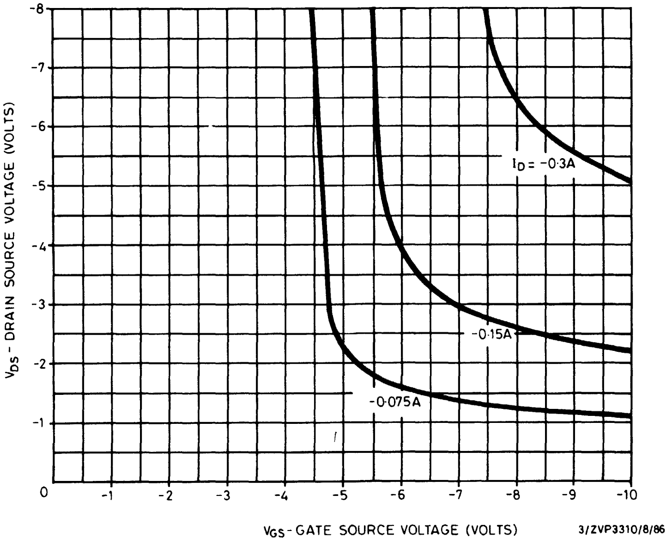


Fig. 3 Typical voltage saturation characteristics

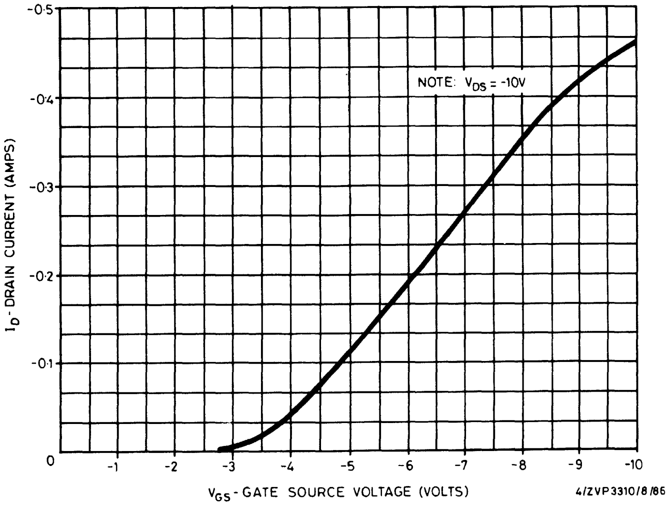
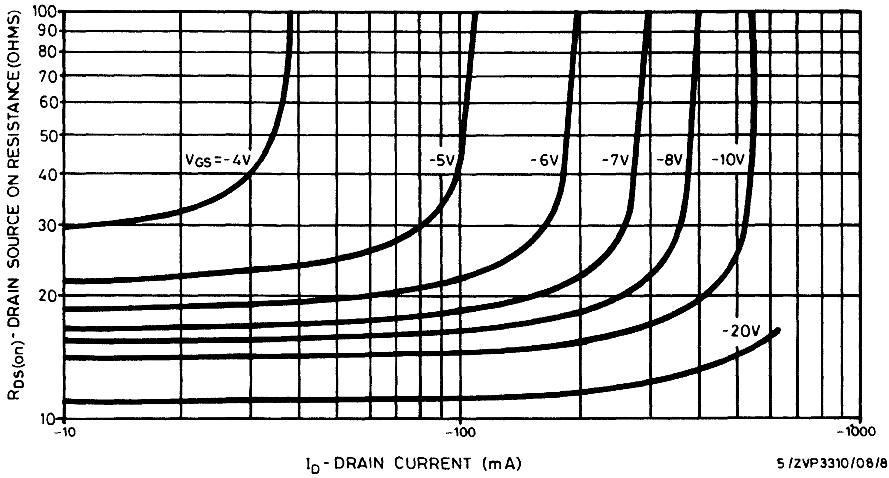
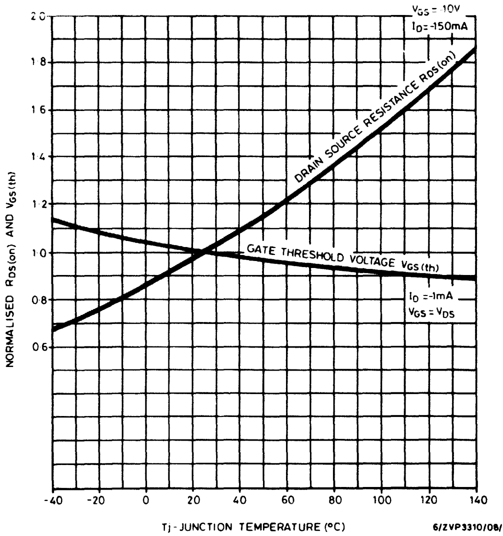


Fig. 4 Typical transfer characteristics



5/ZVP3310/08/86

Fig. 5 Typical on-resistance v drain current



6/ZVP3310/08/86

Fig. 6 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

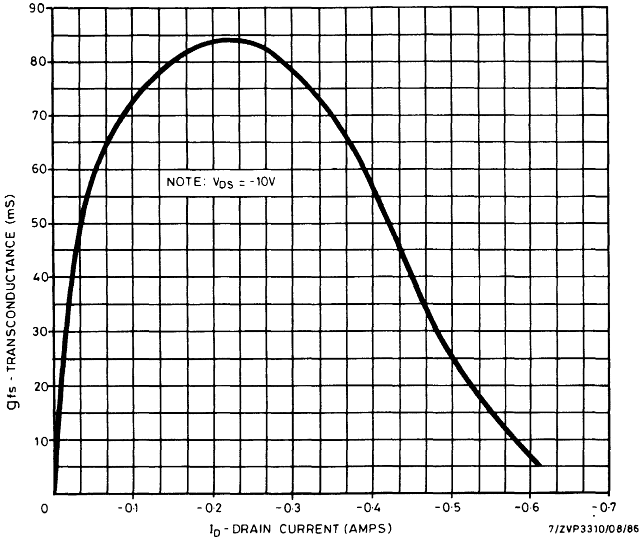


Fig. 7 Typical transconductance v drain current

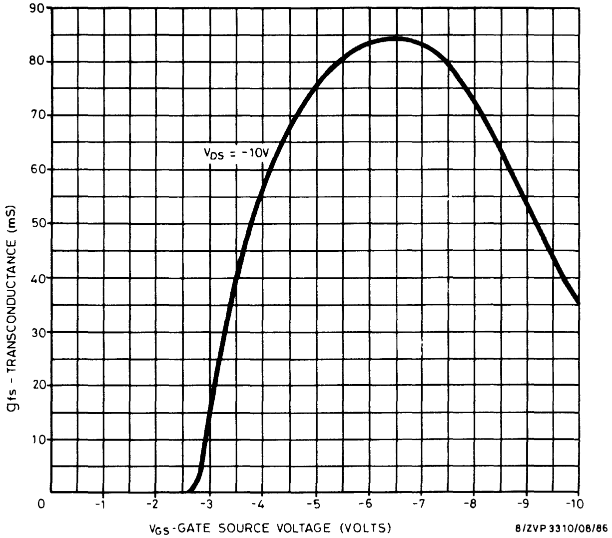


Fig. 8 Typical transconductance v gate-source voltage

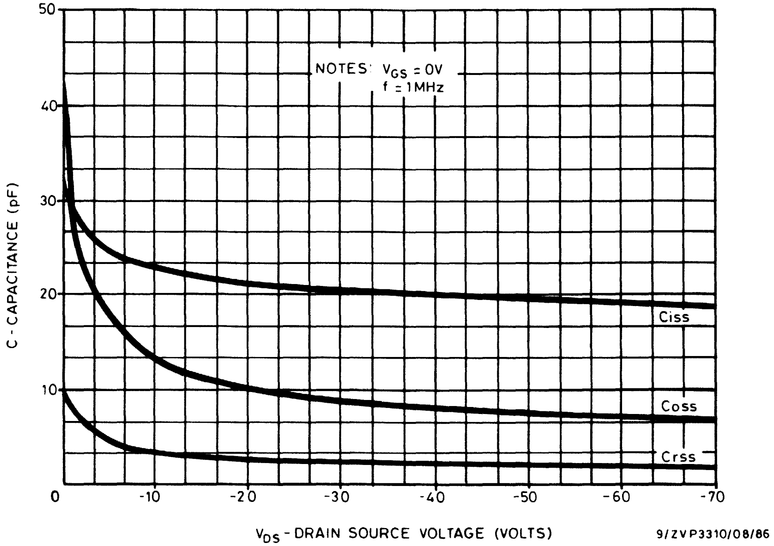


Fig. 9 Typical capacitance v drain-source voltage

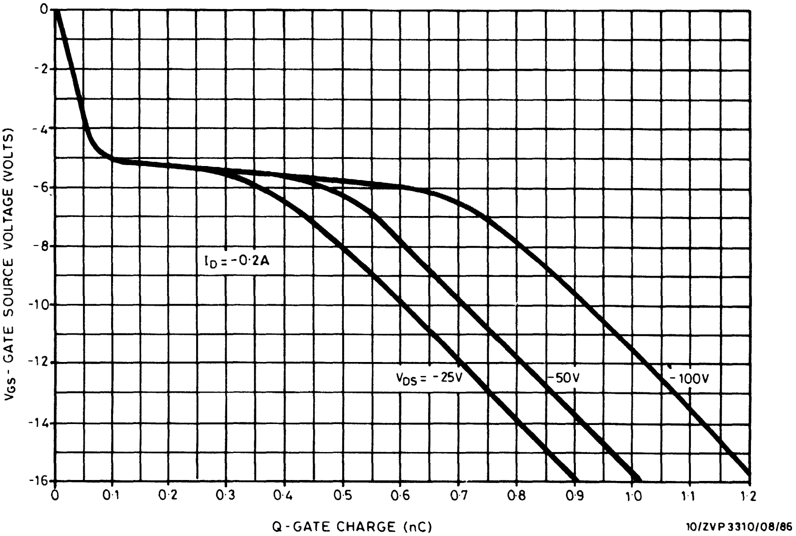


Fig. 10 Typical gate charge v gate-source voltage

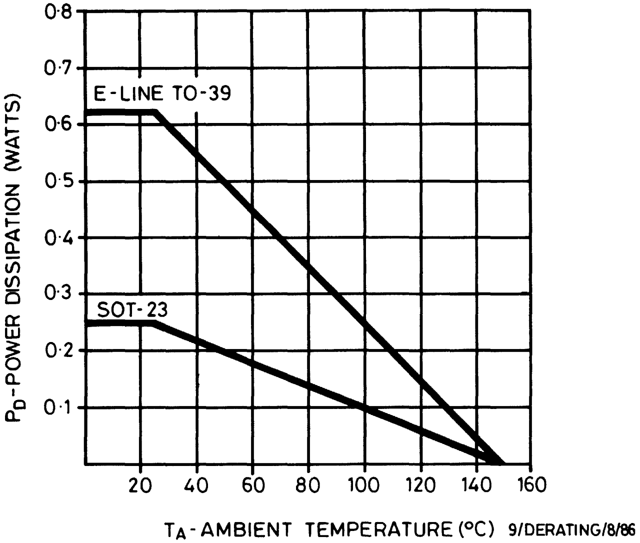


Fig. 11 Power v temperature derating curve (ambient)

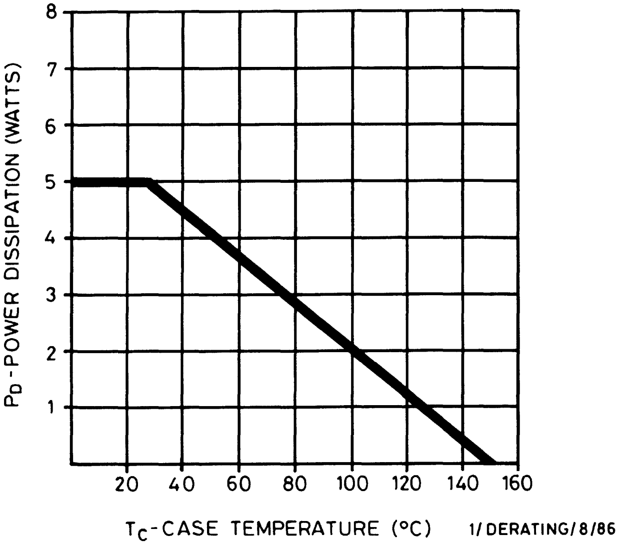


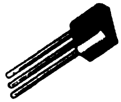
Fig. 12 Power v temperature derating curve (case)

P-channel enhancement mode vertical DMOS FET

ZVP4105

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)
SUFFIX A

DESCRIPTION

A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVP4105A	−50V	−175mA	10Ω

ZVP4105

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	Unit
V_{DS}	Drain-source voltage	−50	V
I_D	Continuous drain current (@ $T_A = 25°C$)	−175	mA
I_{DM}	Pulsed drain current	−520	mA
V_{GS}	Gate-source voltage	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.625	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25°C$ unless otherwise stated).

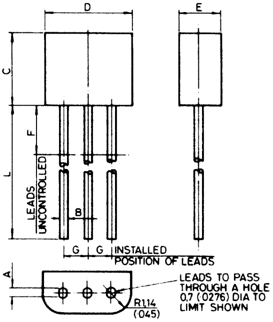
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-source breakdown voltage	BV_{DSS}	−50	—	—	V	$V_{GS} = 0V$ $I_D = -0.25mA$
Gate-source threshold voltage	$V_{GS(th)}$	−0.8	−1.5	−2.0	V	$V_{DS} = V_{GS}$ $I_D = -1mA$
Zero gate voltage drain current	I_{DSS}	—	−1	−15	μA	$T_j = 25°C$
		—	−2	−60	μA	$T_j = 125°C$ $V_{DS} = -50V$, $V_{GS} = 0V$ (2)
		—	—	−100	nA	$T_j = 25°C$ $V_{DS} = -25V$, $V_{GS} = 0V$
Gate-source leakage current	I_{GSS}	—	−1	−10	nA	$V_{GS} = \pm 20V$ $V_{DS} = 0V$
Drain-source on-state resistance (1)	$R_{DS(on)}$	—	6	10	Ω	$V_{GS} = -5V$ $I_D = -100mA$
Forward transconductance (1) (2)	g_{fs}	0.05	0.07	—	S	$V_{DS} = -25V$ $I_D = -100mA$
Input capacitance (2)	C_{iss}	—	40	—	pF	$V_{GS} = 0V$
Output capacitance (2)	C_{oss}	—	15	—		$V_{DS} = -25V$
Reverse transfer capacitance (2)	C_{rss}	—	6	—		$f = 1 MHz$
Turn-on time t_{on}	$t_{d(on)}$	—	10	—	ns	$V_{DD} = -30V$
($t_{on} = t_{d(on)} + t_r$) (2)	t_r	—	10	—		$I_D = -0.27A$
Turn-off time t_{off}	$t_{d(off)}$	—	18	—		$V_{GS} = -5V$
($t_{off} = t_{d(off)} + t_f$) (2)	t_f	—	25	—		$R_{GS} = 50Ω$

Notes: (1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.
(2) Sample test.

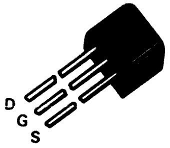
PACKAGE OUTLINE
AND
PIN OUT

PACKAGE DETAILS

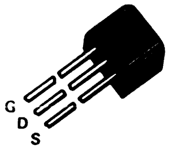
E-LINE



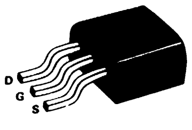
DIMENSION	MILLIMETRES		INCHES	
	MIN	MAX	MIN	MAX
A	0.41	0.495	0.016	0.0195
B	0.41	0.495	0.016	0.0195
C	3.61	4.01	0.142	0.158
D	4.37	4.77	0.172	0.188
E	2.16	2.41	0.085	0.095
F		2.5		0.098
G	1.27 NOM		0.050 NOM	
L	12.06	13.97	0.475	0.550



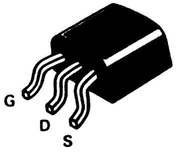
E-LINE
(TO-92 compatible)



E-LINE
(Centre drain configuration)



E-LINE
with M1 lead form

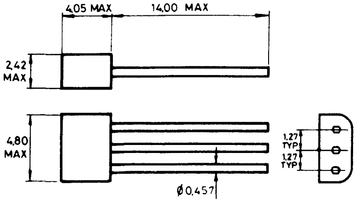


E-LINE 'SM'
(SOT-89 pin compatible)

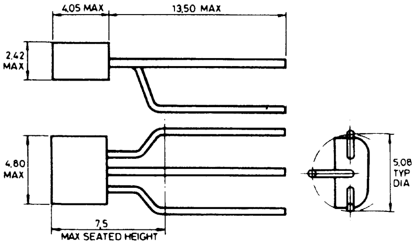
PACKAGE DETAILS

E-LINE (TO-92 STYLE) PACKAGE OUTLINES

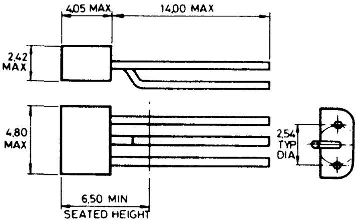
Devices can be ordered with the following lead configurations by adding the indicated suffix to the part number.



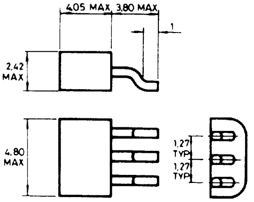
STANDARD PACKAGE
BS3934 SO-94



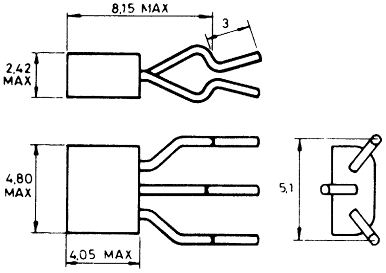
SUFFIX 'K' LEAD FORMATION
for TO-5 and TO-39 compatibility
BS3934 SO-95



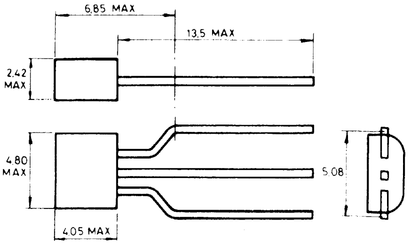
SUFFIX 'L' LEAD FORMATION
for TO-18 compatibility
BS3934 SO-97



SUFFIX 'M1' LEAD FORMATION
for flat mounting
BS3934 SO-96



SUFFIX 'Q' LEAD FORMATION
(Lockfit)



SUFFIX 'S' LEAD FORMATION

Dimensions in millimetres

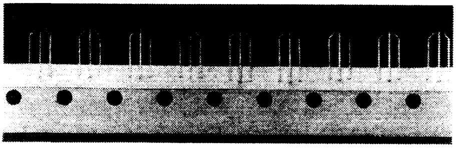
The 'S' type lead formation is pin compatible with the popular TO-202 Plastic Power Transistor

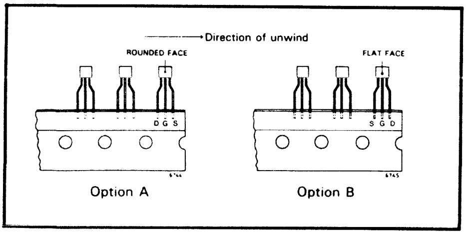
E-LINE TAPING OPTIONS

RADIAL TAPE FOR AUTOMATIC INSERTION

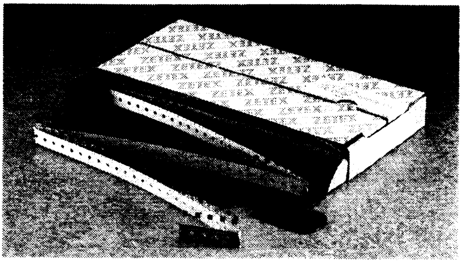
Two types are available.

(a) The tape, bearing the devices, is wound on a reel and supplied in a cardboard box.





(b) The tape, bearing the devices, is folded in a concertina (or Z) form and supplied in a cardboard box (ammo pack).



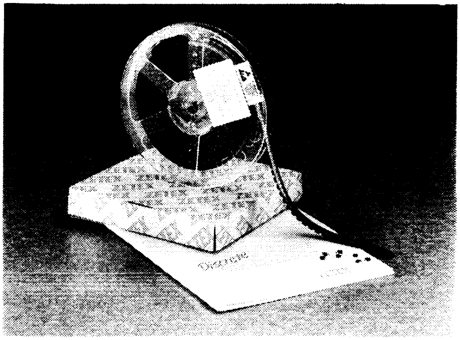
TAPE FEATURES

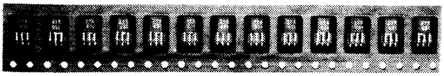
- Each reel or box contains 2,000 devices.
- No more than 2 consecutive vacant spaces on the tape.
- Minimum of 5 vacant spaces at beginning and end of tape.
- Available with choice of orientation.

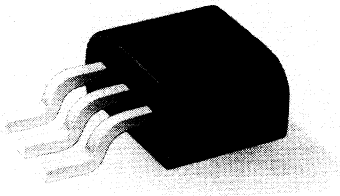
To order E-Line transistors on tape, the following format should be used.

(a) Suffix 'STO' for product taped and put on reels.
(b) Orientation (option A or B).
E.g. ZVN2110ASTOA.
(c) Suffix 'STZ' for product taped and folded (ammo pack). E.g. ZVN2110ASTZ.

M1 IN TAPE FOR SURFACE MOUNTING







TAPE FEATURES

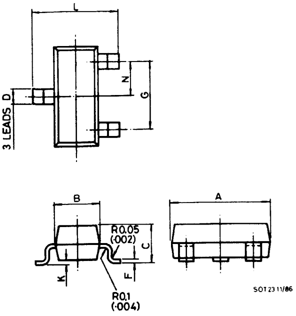
- 13″ reel contains 3,000 devices.
- 7″ reel contains 500 devices.
- Devices contained in anti-static tape.

To order E-Line M1 transistors on tape.

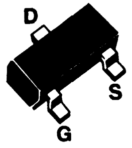
(a) 7″ reels – Suffix device type with M1TA.
E.g. ZVN2110AM1TA.
(b) 13″ reels – Suffix device type with M1TC.
E.g. ZVN2110AM1TC.

PACKAGE DETAILS

SOT-23



DIMENSION	MILLIMETRES		INCHES	
	MIN	MAX	MIN	MAX
A	2.67	3.05	0.105	0.120
B	1.20	1.40	0.047	0.055
C	–	1.10	–	0.043
D	0.37	0.53	0.0145	0.021
F	0.085	0.15	0.0033	0.0059
G	NOM 1.9		NOM 0.075	
K	0.01	0.10	0.0004	0.004
L	2.10	2.5	0.0825	0.0985
N	NOM 0.95		NOM 0.037	

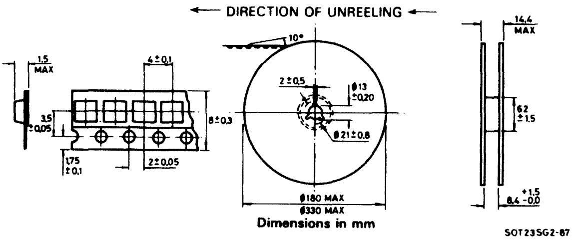


PIN CONFIGURATION

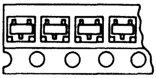
PACKAGE DETAILS

The complete range of SOT-23 devices is now available on Super 8 tape for use with automatic placement equipment. Tape packaging also has special attractions for customers using manual placement since it makes it easier to assemble and orientate these tiny components; stock accounting is also simplified.

Tape specifications



- **Robust antistatic plastic tape**
- **3,000 components per 7″ reel**
  10,000 components per 13″ reel
- **0.25% allowable missing devices/tape**
- **100 min spaces at start and end of the reel.**
- **Complies with both EIA-481 and IEC 286 Industry Standard Specifications**
- **There will be no consecutive missing components before the first and last component on the reel**



OPTION 'A' (THE INDUSTRY STANDARD)

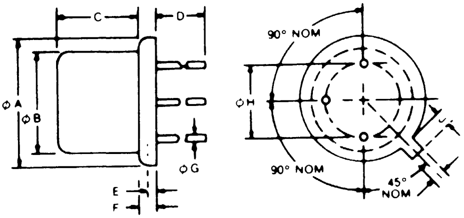
*Ordering format

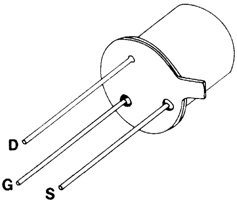
Suffix "T" followed by A to indicate option above on 7″ Reels. E.g. ZVN3306FTA.

Suffix "T" followed by C to indicate option above on 13″ Reels. E.g. ZVN3306FTC.

PACKAGE DETAILS

TO-39



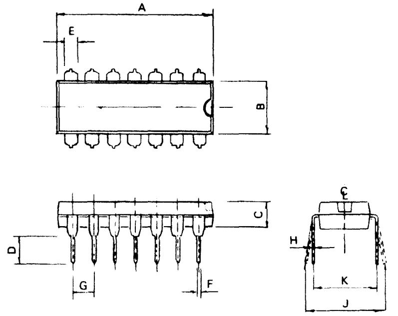


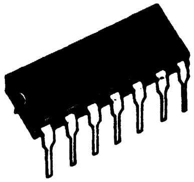
PIN CONFIGURATION

DIMENSION	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
∅A	0.350	0.370	8.99	9.40
∅B	0.306	0.335	7.77	8.51
C	0.240	0.260	6.10	6.60
D	0.500		12.70	
E	0.009	0.023	0.229	0.548
F	0.018	0.045	0.458	1.143
∅G	0.016	0.021	0.406	0.533
∅H	0.190	0.210	4.83	5.33
I	0.028	0.037	0.711	0.939
J	0.026	0.040	0.660	1.016

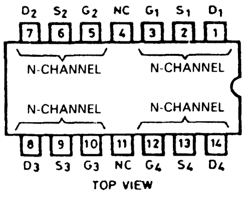
PACKAGE DETAILS

14 LEAD MOULDED DIL

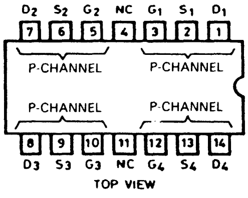




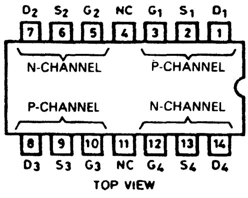
DIM	Millimetres		Inches	
	Min.	Max.	Min.	Max.
A	18.95	19.15	0.746	0.754
B	6.25	6.45	0.246	0.254
C	3.20	3.40	0.126	0.134
D	2.92	3.43	0.115	0.135
E	1.47	1.58	0.058	0.062
F	0.41	0.51	0.016	0.020
G	2.49	2.59	0.098	0.102
H	0.20	0.31	0.008	0.012
J	8.13	9.40	0.320	0.370
K	7.49	8.13	0.295	0.320



4 × N-channel



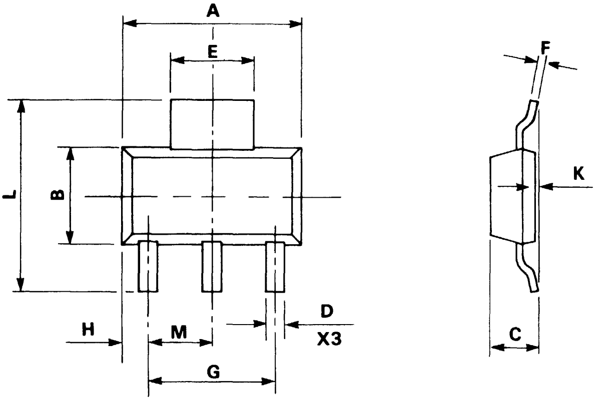
4 × P-channel



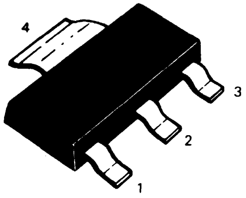
2 × N-channel
2 × P-channel

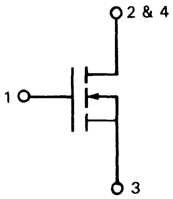
PACKAGE DETAILS

SOT-223



DIM	Millimetres		Inches	
	Min.	**Max.**	**Min.**	**Max.**
A	6.3	6.7	0.248	0.264
B	3.3	3.7	0.130	0.146
C	–	1.7	–	0.067
D	0.6	0.8	0.024	0.031
E	2.9	3.1	0.114	0.122
F	0.24	0.32	0.009	0.013
G	4.6 NOM		0.181 NOM	
H	0.85	1.05	0.033	0.041
K	0.02	0.10	0.0008	0.004
L	6.7	7.3	0.264	0.287
M	2.3 NOM		0.0905 NOM	





1 GATE
2 DRAIN
3 SOURCE
4 DRAIN

PACKAGE DETAILS

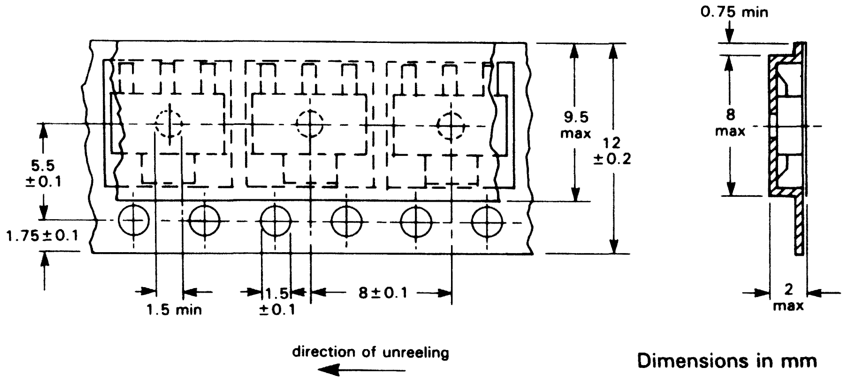
SOT-223

TAPE AND REEL INFORMATION

The complete range of SOT-223 devices is available on 12mm tape for use with automatic placement equipment. Available on either 7in. or 13in. reels, ordering information is as follows:

e.g. ZVN2106GTA 7in. reel 1000 components/reel.
ZVN2106GTC 13in. reel 2500 components/reel.

Tape Specification

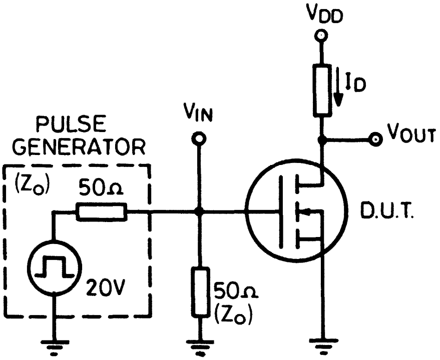


Dimensions in mm

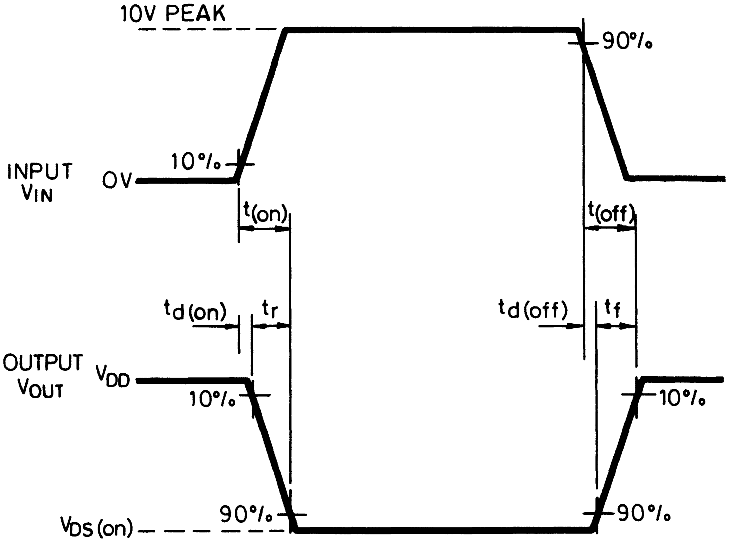
SWITCHING CIRCUITS
AND
WAVEFORMS

SWITCHING

N-channel



Circuit for measuring switching speed

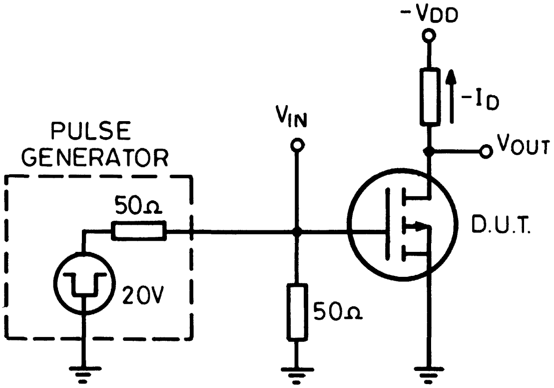


N/MOS/H/B/08/86

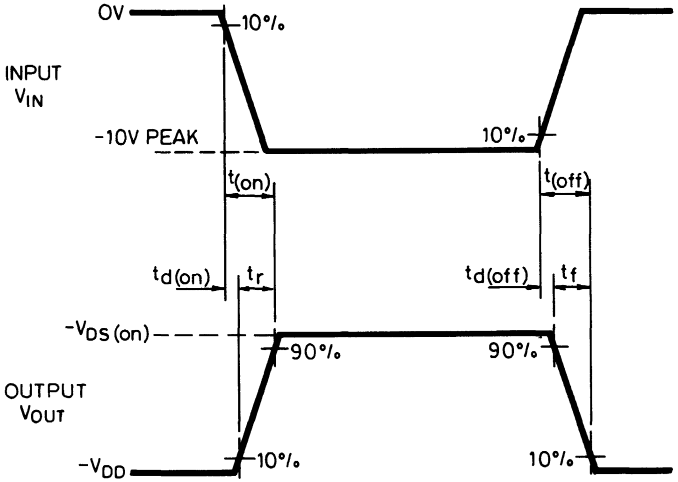
Waveforms

SWITCHING

P-channel



Circuit for measuring switching speed



P/MOS/H/B/08/86

Waveforms

Zetex plc
Fields New Road, Chadderton, Oldham, OL9 8NP, United Kingdom
Telephone: 061-627 5105 (Sales), 061-627 4963 (General Enquiries)
Facsimile: 061-627 5467 Telex: 668038

A Telemetrix PLC Group Company

Zetex GmbH
Drosselweg 30, 8000 München 82
Telefon: (089) 430 90 29 Fax: (089) 439 37 64

Zetex Inc.
87 Modular Avenue, Commack NY11725
Telephone: (516) 543-7100 Fax: (516) 864-7630

Zetex (Asia) Ltd.
47 Seabee Lane, Discovery Bay, Hong Kong
Telephone: 987 9555 Fax: 987 9595

ZETEX